Service Manual

Model : LG-T310i

Internal Use Only

Service Manual

LG-T310i

Date: September, 2010 / Issue 1.0

Table Of Contents

1. INTRODUCTION

1.1 Purpose

This manual provides the information necessary to repair, calibration, description and download the features of this model.

1.2 Regulatory Information

A. Security

Toll fraud, the unauthorized use of telecommunications system by an unauthorized part (for example, persons other than your company's employees, agents, subcontractors, or person working on your company's behalf) can result in substantial additional charges for your telecommunications services. System users are responsible for the security of own system. There are may be risks of toll fraud associated with your telecommunications system. System users are responsible for programming and configuring the equipment to prevent unauthorized use. The manufacturer does not warrant that this product is immune from the above case but will prevent unauthorized use of common-carrier telecommunication service of facilities accessed through or connected to it.

The manufacturer will not be responsible for any charges that result from such unauthorized use.

B. Incidence of Harm

If a telephone company determines that the equipment provided to customer is faulty and possibly causing harm or interruption in service to the telephone network, it should disconnect telephone service until repair can be done. A telephone company may temporarily disconnect service as long as repair is not done.

C. Changes in Service

A local telephone company may make changes in its communications facilities or procedure. If these changes could reasonably be expected to affect the use of the this phone or compatibility with the network, the telephone company is required to give advanced written notice to the user, allowing the user to take appropriate steps to maintain telephone service.

D. Maintenance Limitations

Maintenance limitations on this model must be performed only by the manufacturer or its authorized agent. The user may not make any changes and/or repairs expect as specifically noted in this manual. Therefore, note that unauthorized alternations or repair may affect the regulatory status of the system and may void any remaining warranty.

E. Notice of Radiated Emissions

This model complies with rules regarding radiation and radio frequency emission as defined by local regulatory agencies. In accordance with these agencies, you may be required to provide information such as the following to the end user.

F. Pictures

The pictures in this manual are for illustrative purposes only; your actual hardware may look slightly different.

G. Interference and Attenuation

Phone may interfere with sensitive laboratory equipment, medical equipment, etc.Interference from unsuppressed engines or electric motors may cause problems.

H. Electrostatic Sensitive Devices

ATTENTION

Boards, which contain Electrostatic Sensitive Device (ESD), are indicated  **by the sign. Following information is ESD handling:**

- Service personnel should ground themselves by using a wrist strap when exchange system boards.
- When repairs are made to a system board, they should spread the floor with anti-static mat which is also grounded.
- Use a suitable, grounded soldering iron.
- Keep sensitive parts in these protective packages until these are used.
- When returning system boards or parts like EEPROM to the factory, use the protective package as described.

1.3 Abbreviations

For the purposes of this manual, following abbreviations apply:

APC	Automatic Power Control
BB	Baseband
BER	Bit Error Ratio
CC-CV	Constant Current – Constant Voltage
DAC	Digital to Analog Converter
DCS	Digital Communication System
dBm	dB relative to 1 milli watt
DSP	Digital Signal Processing
EEPROM	Electrical Erasable Programmable Read-Only Memory
ESD	Electrostatic Discharge
FPCB	Flexible Printed Circuit Board
GMSK	Gaussian Minimum Shift Keying
GPIB	General Purpose Interface Bus
GSM	Global System for Mobile Communications
IPUI	International Portable User Identity
IF	Intermediate Frequency
LCD	Liquid Crystal Display
LDO	Low Drop Output
LED	Light Emitting Diode
OPLL	Offset Phase Locked Loop

PAM	Power Amplifier Module
PCB	Printed Circuit Board
PGA	Programmable Gain Amplifier
PLL	Phase Locked Loop
PSTN	Public Switched Telephone Network
RF	Radio Frequency
RLR	Receiving Loudness Rating
RMS	Root Mean Square
RTC	Real Time Clock
SAW	Surface Acoustic Wave
SIM	Subscriber Identity Module
SLR	Sending Loudness Rating
SRAM	Static Random Access Memory
PSRAM	Pseudo SRAM
STMR	Side Tone Masking Rating
TA	Travel Adapter
TDD	Time Division Duplex
TDMA	Time Division Multiple Access
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator
VCTCXO	Voltage Control Temperature Compensated Crystal Oscillator
WAP	Wireless Application Protocol

2. PERFORMANCE

2.1 H/W Features

Item	Feature	Comment
Standard Battery	Lithium-Ion, 3.7V 900mAh	
Stand by TIME	Up to 350 hrs : Paging Period 5, RSSI 85dBm	
Talk time	Up to 200min : GSM Tx Level 7	
Stand by time	Up to 350 hours (Paging Period: 5, RSSI: -85 dBm)	
Charging time	Approx. 2.5 hours	
RX Sensitivity	GSM, EGSM: -109dBm, DCS: -109dBm	
TX output power	GSM, EGSM: 32.3dBm(Level 5), DCS , PCS: 29.5dBm(Level 0)	
GPRS compatibility	Class 10	
SIM card type	3V / 1.8V	
Display	MAIN : 2.8" TFT 240 × 320 pixel 262K Color	
Status Indicator	Send Key, End Key, Cancel Key, Volume Up/Down Key, PWR Key,	
ANT	Internal	
EAR Phone Jack	Yes	
PC Synchronization	Yes	
Speech coding	EFR/FR/HR	
Data and Fax	Yes	
Vibrator	Yes	
Loud Speaker	Yes	
Voice Recoding	Yes	
Microphone	Yes	

2. PERFORMANCE

Item	Feature	Comment
Speaker/Receiver	18x12Φ Speaker/ Receiver	
Travel Adapter	Yes	
MIDI	SW MIDI (Mono SPK)	
Camera	2.0M FF	
Bluetooth / FM Radio	Bluetooth version 2.1 / 76~108MHz supported	

2.2 Technical Specification

<table>
<tr><th>Item</th><th>Description</th><th>Specification</th></tr>
<tr><td>1</td><td>Frequency Band</td><td>GSM850
TX: 824 ~ 849 MHz
RX: 869 ~ 894 MHz
EGSM
TX: 880 ~ 915MHz
RX: 925 ~ 960 MHz
DCS
TX: 1710 ~ 1785 MHz
RX: 1805 ~ 1880 MHz
PCS
TX: 1850 ~ 1910 MHz
RX: 1930 ~ 1990 MHz</td></tr>
<tr><td>2</td><td>Phase Error</td><td>RMS < 5 degrees
Peak < 20 degrees</td></tr>
<tr><td>3</td><td>Frequency Error</td><td>< 0.1 ppm</td></tr>
<tr><td>4</td><td>Power Level</td><td>
GSM850/EGSM
<table>
<tr><th>Level</th><th>Power</th><th>Toler.</th><th>Level</th><th>Power</th><th>Toler.</th></tr>
<tr><td>5</td><td>33dBm</td><td>±2dB</td><td>13</td><td>17dBm</td><td>± 3dB</td></tr>
<tr><td>6</td><td>31dBm</td><td>±3dB</td><td>14</td><td>15dBm</td><td>± 3dB</td></tr>
<tr><td>7</td><td>29dBm</td><td>±3dB</td><td>15</td><td>13dBm</td><td>± 3dB</td></tr>
<tr><td>8</td><td>27dBm</td><td>±3dB</td><td>16</td><td>11dBm</td><td>± 5dB</td></tr>
<tr><td>9</td><td>25dBm</td><td>±3dB</td><td>17</td><td>9dBm</td><td>± 5dB</td></tr>
<tr><td>10</td><td>23dBm</td><td>±3dB</td><td>18</td><td>7dBm</td><td>± 5dB</td></tr>
<tr><td>11</td><td>21dBm</td><td>±3dB</td><td>19</td><td>5dBm</td><td>± 5dB</td></tr>
<tr><td>12</td><td>19dBm</td><td>±3dB</td><td></td><td></td><td></td></tr>
</table>
DCS/PCS
<table>
<tr><th>Level</th><th>Power</th><th>Toler.</th><th>Level</th><th>Power</th><th>Toler.</th></tr>
<tr><td>0</td><td>30dBm</td><td>±2dB</td><td>8</td><td>14dBm</td><td>± 3dB</td></tr>
<tr><td>1</td><td>28dBm</td><td>±3dB</td><td>9</td><td>12dBm</td><td>± 4dB</td></tr>
<tr><td>2</td><td>26dBm</td><td>±3dB</td><td>10</td><td>10dBm</td><td>± 4dB</td></tr>
<tr><td>3</td><td>24dBm</td><td>±3dB</td><td>11</td><td>8dBm</td><td>± 4dB</td></tr>
<tr><td>4</td><td>22dBm</td><td>±3dB</td><td>12</td><td>6dBm</td><td>± 4dB</td></tr>
<tr><td>5</td><td>20dBm</td><td>±3dB</td><td>13</td><td>4dBm</td><td>± 4dB</td></tr>
<tr><td>6</td><td>18dBm</td><td>±3dB</td><td>14</td><td>2dBm</td><td>± 5dB</td></tr>
<tr><td>7</td><td>16dBm</td><td>±3dB</td><td>15</td><td>0dBm</td><td>± 5dB</td></tr>
</table>
</td></tr>
</table>

2. PERFORMANCE

Item	Description	Specification	
5	Output RF Spectrum (due to modulation)	**GSM850/ EGSM**	
		Offset from Carrier (kHz).	Max. dBc
		100	+0.5
		200	-30
		250	-33
		400	-60
		600~ <1,200	-60
		1,200~ <1,800	-60
		1,800~ <3,000	-63
		3,000~ <6,000	-65
		6,000	-71
		DCS/PCS	
		Offset from Carrier (kHz).	Max. dBc
		100	+0.5
		200	-30
		250	-33
		400	-60
		600~ <1,200	-60
		1,200~ <1,800	-60
		1,800~ <3,000	-65
		3,000~ <6,000	-65
		6,000	-73
6	Output RF Spectrum (due to switching transient)	**GSM850/ EGSM**	
		Offset from Carrier (kHz).	Max. dBm
		400	-19
		600	-21
		1,200	-21
		1,800	-24

<table>
<tr><th>Item</th><th>Description</th><th colspan="3">Specification</th></tr>
<tr><td rowspan="6">6</td><td rowspan="6">Output RF Spectrum
(due to switching
transient)</td><td colspan="3">DCS/PCS</td></tr>
<tr><td colspan="2">Offset from Carrier (kHz).</td><td>Max. dBm</td></tr>
<tr><td colspan="2">400</td><td>-22</td></tr>
<tr><td colspan="2">600</td><td>-24</td></tr>
<tr><td colspan="2">1,200</td><td>-24</td></tr>
<tr><td colspan="2">1,800</td><td>-27</td></tr>
<tr><td>7</td><td>Spurious Emissions</td><td colspan="3">Conduction, Emission Status</td></tr>
<tr><td>8</td><td>Bit Error Ratio</td><td colspan="3">GSM850, EGSM
BER (Class II) < 2.439% @-102 dBm
DCS,PCS
BER (Class II) < 2.439% @-100 dBm</td></tr>
<tr><td>9</td><td>RX Level Report Accuracy</td><td colspan="3">±3 dB</td></tr>
<tr><td>10</td><td>SLR</td><td colspan="3">12±3 dB</td></tr>
<tr><td rowspan="10">11</td><td rowspan="10">Sending Response</td><td>Frequency (Hz)</td><td>Max.(dB)</td><td>Min.(dB)</td></tr>
<tr><td>100</td><td>-12</td><td>-</td></tr>
<tr><td>200</td><td>0</td><td>-</td></tr>
<tr><td>300</td><td>0</td><td>-12</td></tr>
<tr><td>1,000</td><td>0</td><td>-6</td></tr>
<tr><td>2,000</td><td>4</td><td>-6</td></tr>
<tr><td>3,000</td><td>4</td><td>-6</td></tr>
<tr><td>3,400</td><td>4</td><td>-9</td></tr>
<tr><td>4,000</td><td>0</td><td>-</td></tr>
<tr><td>12</td><td>RLR</td><td colspan="3">4±3 dB</td></tr>
</table>

2. PERFORMANCE

<table>
<tr><th>Item</th><th>Description</th><th colspan="3">Specification</th></tr>
<tr><td rowspan="11">13</td><td rowspan="11">Receiving Response</td><td>Frequency (Hz)</td><td>Max.(dB)</td><td>Min.(dB)</td></tr>
<tr><td>100</td><td>-12</td><td>-</td></tr>
<tr><td>200</td><td>0</td><td>-</td></tr>
<tr><td>300</td><td>2</td><td>-7</td></tr>
<tr><td>500</td><td>*</td><td>-5</td></tr>
<tr><td>1,000</td><td>0</td><td>-5</td></tr>
<tr><td>3,000</td><td>2</td><td>-5</td></tr>
<tr><td>3,400</td><td>2</td><td>-10</td></tr>
<tr><td>4,000</td><td>2</td><td></td></tr>
<tr><td colspan="3">* Mean that Adopt a straight line in between 300 Hz and 1,000 Hz to be Max. level in the range.</td></tr>
<tr><td>14</td><td>STMR</td><td colspan="3">> 17 dB</td></tr>
<tr><td>15</td><td>Stability Margin</td><td colspan="3">> 6 dB</td></tr>
<tr><td rowspan="9">16</td><td rowspan="9">Distortion</td><td colspan="2">dB to ARL (dB)</td><td>Level Ratio (dB)</td></tr>
<tr><td colspan="2">-35</td><td>17.5</td></tr>
<tr><td colspan="2">-30</td><td>22.5</td></tr>
<tr><td colspan="2">-20</td><td>30.7</td></tr>
<tr><td colspan="2">-10</td><td>33.3</td></tr>
<tr><td colspan="2">0</td><td>33.7</td></tr>
<tr><td colspan="2">7</td><td>31.7</td></tr>
<tr><td colspan="2">10</td><td>25.5</td></tr>
<tr><td>17</td><td>Side Tone Distortion</td><td colspan="3">Three stage distortion < 10%</td></tr>
<tr><td>18</td><td>System frequency (13 MHz) tolerance</td><td colspan="3">≤ 2.5 ppm</td></tr>
<tr><td>19</td><td>32.768KHz tolerance</td><td colspan="3">≤ 30 ppm</td></tr>
<tr><td>20</td><td>Ringer Volume</td><td colspan="3">At least 55 dBspl under below conditions:
1. Ringer set as ringer.
2. Test distance set as 1 m</td></tr>
</table>

<table>
<tr><th>Item</th><th>Description</th><th colspan="3">Specification</th></tr>
<tr><td>21</td><td>Charge Current</td><td colspan="3">Fast Charge : Typ. 400 mA
Slow Charge : Typ. 95mA
Total Charging Time : < 3 hours</td></tr>
<tr><td rowspan="8">22</td><td rowspan="8">Antenna Display</td><td>Bar Number</td><td colspan="2">Power</td></tr>
<tr><td>7</td><td colspan="2">Over -93</td></tr>
<tr><td>7 -> 5</td><td colspan="2">-93 ± 2</td></tr>
<tr><td>5 -> 4</td><td colspan="2">-98 ± 2</td></tr>
<tr><td>4 -> 2</td><td colspan="2">-101 ± 2</td></tr>
<tr><td>2 -> 1</td><td colspan="2">-104 ± 2</td></tr>
<tr><td>1 -> 0</td><td colspan="2">-106 ± 2</td></tr>
<tr><td>0 -> OFF</td><td colspan="2">Under -106</td></tr>
<tr><td rowspan="5">23</td><td rowspan="5">Battery Indicator</td><td colspan="2">Battery Bar Number</td><td>Voltage</td></tr>
<tr><td colspan="2">3</td><td>≥ 3.71± 0.05 V</td></tr>
<tr><td colspan="2">3 -> 2</td><td>3.71 ± 0.05 V</td></tr>
<tr><td colspan="2">2 -> 1</td><td>3.58 ± 0.05 V</td></tr>
<tr><td colspan="2">1 -> 0</td><td>3.45 ± 0.05 V</td></tr>
<tr><td rowspan="2">24</td><td rowspan="2">Low Voltage Warning
(Blinking Bar)</td><td colspan="3">≤ 3.45 ± 0.05V(Call), 1 time per 1 minute (Receiver)</td></tr>
<tr><td colspan="3">≤ 3.45 ± 0.05V(Standby), 1 time per 3 minute (Speaker)</td></tr>
<tr><td>25</td><td>Forced shut down
Voltage</td><td colspan="3">3.35 ± 0.05V</td></tr>
<tr><td>26</td><td>Sustain RTC
without battery</td><td colspan="3">Over 2 hours</td></tr>
<tr><td>27</td><td>Battery Type</td><td colspan="3">Lithium-Ion Battery
Standard Voltage = 3.7 V
Battery full charge voltage = 4.2 V
Capacity: 900mAh</td></tr>
<tr><td>28</td><td>Travel Charger</td><td colspan="3">Switching-mode charger
Input: 100 ~ 240V, 50/60 Hz
Output: 4.8V, 400mA</td></tr>
</table>

3. TECHNICAL BRIEF

3.1 Digital Main Processor

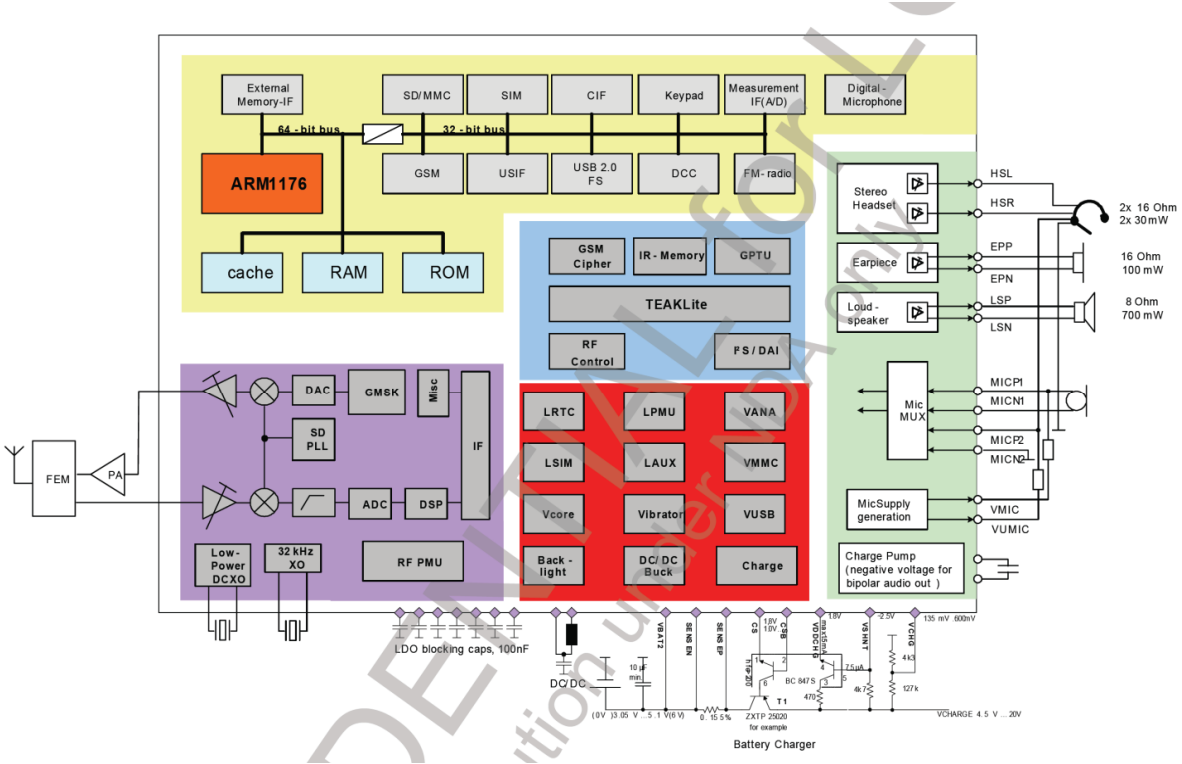


Figure. 3.1.1 X-Gold tm 213 Hardware Block Diagram

3.1.1 General

• Technology:
– SoC, Monolithic, 65 nm CMOS
• Package:
– eWLB, 8x8x0.8 mm
– 0.5 mm pitch
– 217 balls / 8-layer PCB

3.1.2 RF Transceiver

• Dual-band direct conversion receiver
• Tri/Quad-band possible with external circuitry
• Fully integrated digital controlled X0
• Additional buffer for 2 external system clocks
• Fully digital RF-Synthesizer incl. ΣΔ-Transmitter

3.1.3 Baseband

• DSP:
– 156 MHz TeakLite™
• MCU:
– ARM1176® @ 208 MHz
• MCU RAM:
– 3.00Mbit
• Memory I/F:
– 512 Mbit
• Modem:
– GPRS class 12, (RX/TX CS1-CS4)
– EGPRS class 12, (RX MCS1-MCS9, TX MCS1-MCS4)
• Cipher Units:
– A51/2/3
– GEA-1/2/3
• Security:
– OMTP TR0
– Secure Boot
– RSA(ROM)/SHA-1(HW accel.)
– OCDS disabling
– Certificate Management

• Speech Codec:
– FR / HR / EFR / NB-AMR
• Audio Codec (running on ARM1176):
– SP-MIDI
– SB-ADPCM
– MP3
– WB-AMR
– AAC/AAC+/eAAC+
• Others:
– DARP (SAIC)
– TTY
• Customization:
– E-Fuses

3.1.4 External Memory

• External Bus Unit
– 25-bit address bus (512 Mbit)
– 16-bit data bus
– 1.8V & 2.8V support
• Flash / RAM
– NOR Type
– Serial Flash SPI and SPI-4
– Parallel Flash (Page & Burst Mode)
- 16-bit Demultiplexed
- 16-bit AD-multiplexed
- 16-bit AAD-multiplexed
– iNAND Type e.g. oneNAND
• Memory card
– SD/MMC card interface with 1 or 4 data lines

3.1.5 Connectivity

• 3xUSIF (configurable either as SPI or UART), I2C, I2S; Interfaces @ 1.8V
• Direct (U)SIM 1.8/3V
• USB2.0 up to 480 Mbit/s (High Speed) w/ external USB Phy over ULPI interface
• Stereo Headset (Amplifier integrated)
• 3 external analog measurement PIN's
• Bluetooth

3.1.6 Mixed Signal

• Improved audio performance
• Loudspeaker Audio Class D Amplifier, 700 mW@8 Ω mono for hands-free and ringing
• Stereo Headset 2x30 mW@16 Ω w/o coupling C
• Mono Earpiece 100 mW@16 Ω
• Digital microphone supported
• Differential microphone inputs

3.1.7 FM Radio

• Integrated FM radio
– FM Stereo RDS Receiver
– Sensitivity 2 µV EMF
– Support for US & EU bands
– Stereo recording

3.1.8 Power Management

• Direct-to-Battery Connection
– LDOs (incl. capless)
– DC/DC step-down converter
– DC/DC step-up for white LED supply
• Battery Type
– Li-Polymer
• Charging control
– Battery temperature
– Watchdog protection
– Start-up on flat battery
• External Charger
– Switch mode
• USB battery charging
– USB charging spec 1.0 compliant
• Backlight
– Up to 4 serial white LEDs (integrated LDO)

3.1.9 Main LCD Display

• Type
– 240*320, QCIF, 262k color (parallel)
• Interface
– 80 Series Parallel 8bit
– Interf. voltage at 1.8V
• gRacr - Display Controller (Hardware)
– 30 fps Display update without DMA (up to 60 fps) (full or partial)
– Video post processing Scaling, Rotation (90° steps), Mirroring
– Overlay with alpha blending
– Color conversion YUV -> RGB
– 2D vector graphics (Lines, filled rectangles, Bit block transfer (e.g. sprites, scrolling, antialiased bitmap fonts)

3.1.10 Camera

• 2.0 Mpxls, FF
• Frame Rate : 15@UXGA, 30@SVGA
• 39 MHz Pixel Rate
• 15 fps@1.3 Mpx full resolution

3.1.11 Video Capabilities

• Video Decoding MPEG-4/H.263
– QCIF@30 fps
– QVGA@15fps
• Video Encoding MPEG-4/H.263
– QCIF@15 fps

3.1.12 Audio Capabilities

• Polyphonic ring tones
– 64 voices MIDI, SP-MIDI
– FM synthesizer
• AMR-WB
• True ring tones (MP3)
• MP3, eAAC+
• G.722 SB-ADPCM encoding/decoding

3.2 Power Management

A mobile platform requires power supplies for different functions. These power supplies are generated in the integrated power management Unit (PMU). The PMU is designed to deliver the power for a typical standard phone.

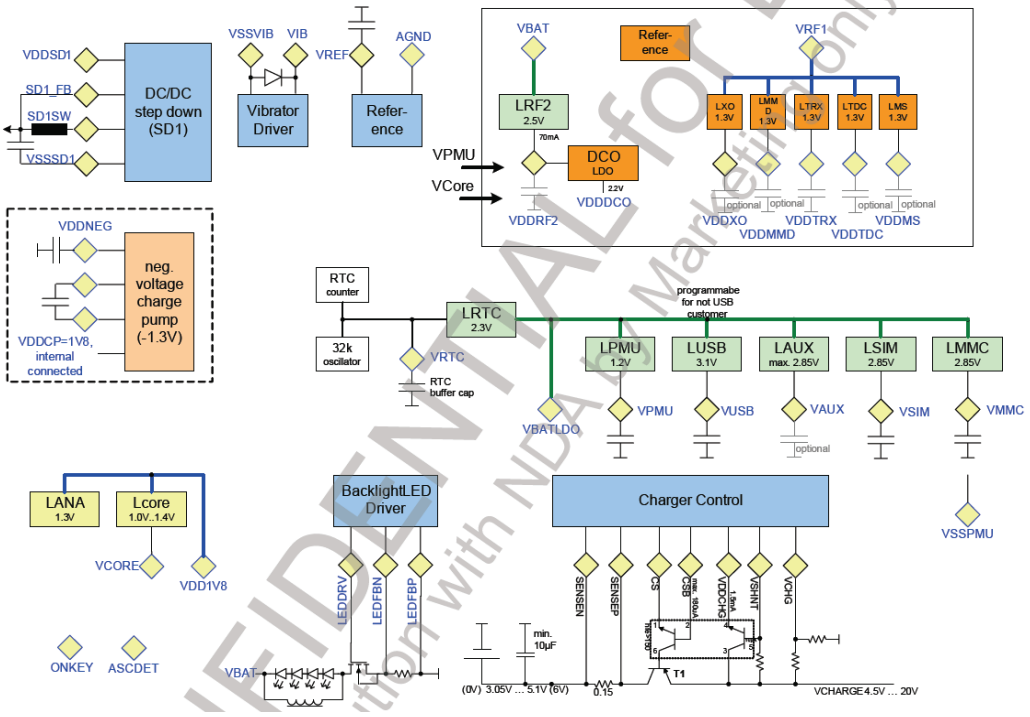


Figure. 3-2-1 Block Figure of the PMU Modules X-Gold tm 213

▪ **DC/DC Step Down Converter for 1.8V (SD1)**
The DC/DC converter generates a 1.8V supply rail. This voltage rail is used to supply main parts of the system, like the digital core of the chip (via LDO LCORE), some parts of the mixed signal macro, parts of the RF macro and the external memory if a 1.8V memory is used. The efficiency of the DC/DC converter is optimized for an average load current of 100mA. That is the load current estimated for the GSM talk mode.

▪ **Linear voltage Regulators (low dropout) LDOs**
The LDOs are used to generate the supply for the different supply domains not directly supplied out of the DC/DC converter.
The VSIM output current is high enough to drive USB SIM cards.

▪ **LCORE**
The LCORE LDO provides the VCORE supply used for most of the digital parts of the chip

▪ **LPMU**
The LPMU provides VPMU sued for the PMU supply, e.g. for the startup state machine and analog parts like ADC, sense amplifier etc.

▪ **LUSB**
The LUSB LDO generates the supply for the USB transceiver (output driver and input). If no USB interface is required, LUSB can be used as general purpose LDO.

▪ **LAUX**
The LAUX generates VAUX. It is a general purpose LDO and can be used for different functions depending on the phone application, e.g. for the display or Camera.

▪ **LMMC**
The LMMC generates VMMC. It is a general purpose LDO and can be used e,g. for memory cards

▪ **LSIM**
The LSIM LDO generates the VSIM supply for the SIM card and interface. It is designed to supply Standard SIM cards.

▪ **Other LDOs**
The RF module has implemented several LDO's for different RF Power domain.
The mixed signal module has some LDO's for the audio driver and microphone supply.

Supply Domain LDO Name	Voltage	Max. Current	Output Cap	Input Domain	Comment
VBAT	0 ... 6.0 V				Operating range is 3.05 V ... 5.5 V, system emergency switch off voltage is about 2.8 V
VDD1V8	1.8 V	450 mA	22 µF	VBAT	This voltage is generated by the DC/DC converter with 3.3 µH inductor, The voltage is used for: Memory supply, and via LDO's for digital core supply, mixed signal supply and RF supply.
LCORE	1.2 V	300 mA	2x100 nF	VDD1V8	
LANA	1.3 V	10 mA	No	VDD1V8	No ball
LRTC	2.3 V	2 mA	>=100 nF	VBAT	This supply is only used for the HPBG, the 32.768 kHz oscillator and the real-time clock counter required during the sleep- and low-power mode.
LPMU	1.2 V	15 mA	100 nF	VBAT	Supply for the digital part of the PMU including digital control of DC/DC converter. This voltage is also used for the N-DEMOS driver of DC/DC converter and the class-D amplifier and the core PLL.
LUSB	3.1 V	40 mA	100 nF	VBAT	Used for the USB driver supply or as general purpose LDO with programmable output voltages (2.5 V, 2.85 V, 3.1 V)
LAUX	1.5 V ... 2.85 V	150 mA	470 nF	VBAT	General purpose LDO for e.g. Display, Bluetooth, Camera etc. Programmable output voltages are (1.5 V, 1.8 V, 2.5 V, 2.85 V)
LSIM	1.8 V / 2.85 V	30 mA	>=100 nF	VBAT	LDO dedicated to the SIM-Card supply. It is chip internal connected to the SIM interface driver.
LMMC	1.5 V ... 2.85 V	150 mA	>=470 nF	VBAT	General purpose LDO, targeted for MMC/SD card supply.
VDDNEG	-1.3 V	100 mA	100 nF	VDD1V8	Negative voltage for the bipolar headset audio driver. Generated by a charge pump.

Table. 3-2-1 Power supply Domains (without RF)

3.2.1 Power on and startup

- **Analog startup Circuit**

Because the POR circuit and the LPBG are directly connected to the battery, it is not possible to switch them off. If the battery voltage exceed the power on reset threshold (2.5V), the power on reset is released, the LPMU regulator and the LRTC voltage regulator are switched on. The LPMU regulator starts in its ultra-low power mode.

The LPMU regulator generates a control signal (lpmu_OK) that enables the 50KHZ PMU oscillator. The output clock of the oscillator is checked with a fully coded counter. A counter overflow releases the reset (vpmu_rst_n) signal for the small PMU state-machine.

- **Small first digital State-Machine**

The small PMU state-machine is always connected to VPMU After starting from reset the small startup state machine enters the SYSTEM OFF state and only continuous the startup procedure if a switch on event like first connect, on-key, wake up or charge detect occurs.

- **PMU-main State-Machine**

The main PMU state-machine is always connected to VPMU also. The power up sequence driven by the PMU state-machine can be seen in Figure18. After enabling the reference (HPGB) and waiting for the settling time, the battery voltage is measured and compared with the power on threshold. If the battery voltage is high enough, the SD1 DC/DC converter and the LCORE LDO are started. A timer ensures that the supply voltage will be stable before the DCXO is enabled. The DCXO settling time is ensured using a fixed timer. After an overflow of this timer, the reset is released for the rest of the system. The PMU state machine remains in this System-ON state until the system is switched into the OFF state. For example the system sleep mode is completely configured by software(for example switching off the LDO's, switching of the DCXO etc.) and controlled by the VCXO_enable signal. The reason for the startup is stored in the ResetSourceRead register.

- **Battery Measurement**

The ADC and the oscillator for the ADC needs the VDD_ADC supply voltage from the LADC LDO. LADC uses either the charger voltage VDD_CHARGE or VDDRTC as input voltage. The input voltage is selected automatically by a bulk switch circuit. LADC, the ADC and the oscillator are enabled on request for every battery measurement if the charger unit is not running. This is handled by an ADC control block in one of the state-machines. If the charger unit is running the ADC is controlled by the charger state-machine

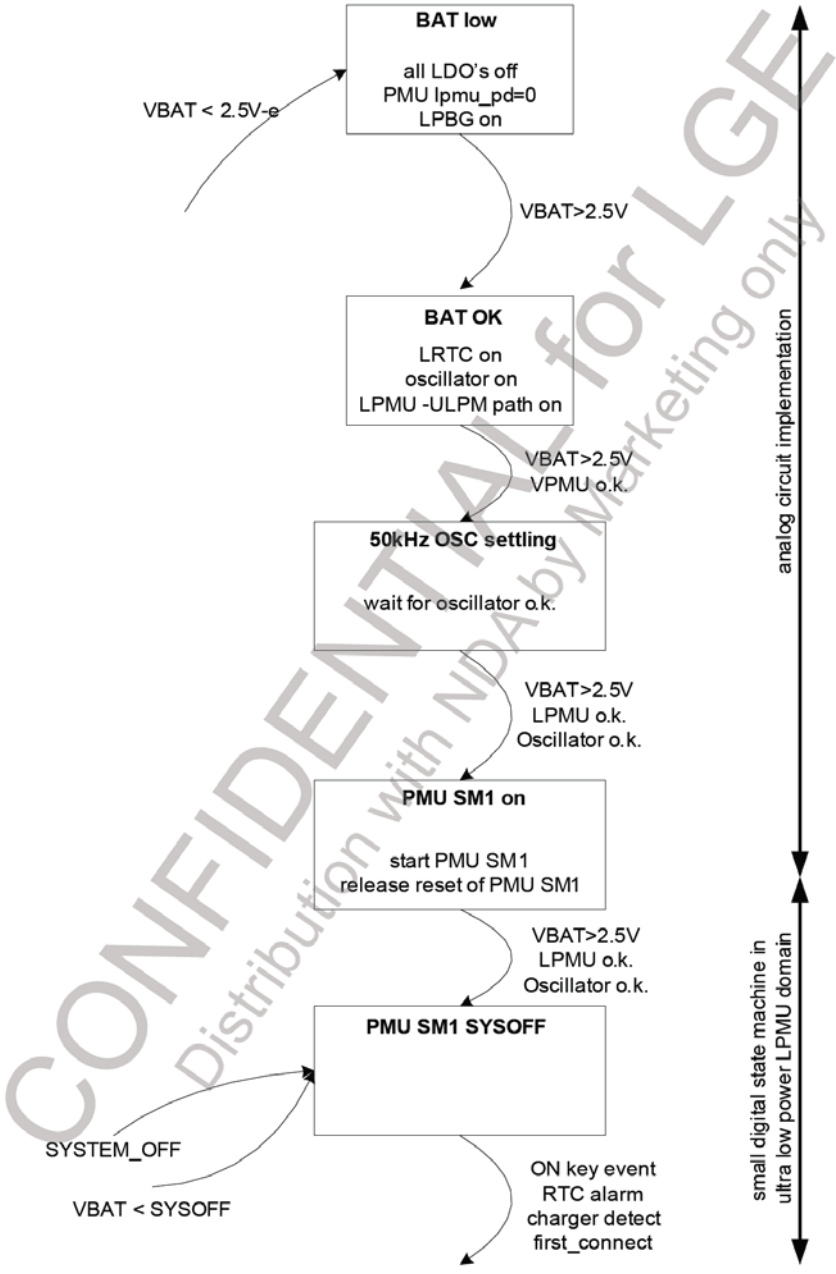


Figure.3.2.1 First Part of the State Machine,
Running in Different Power Domains than the Second Part

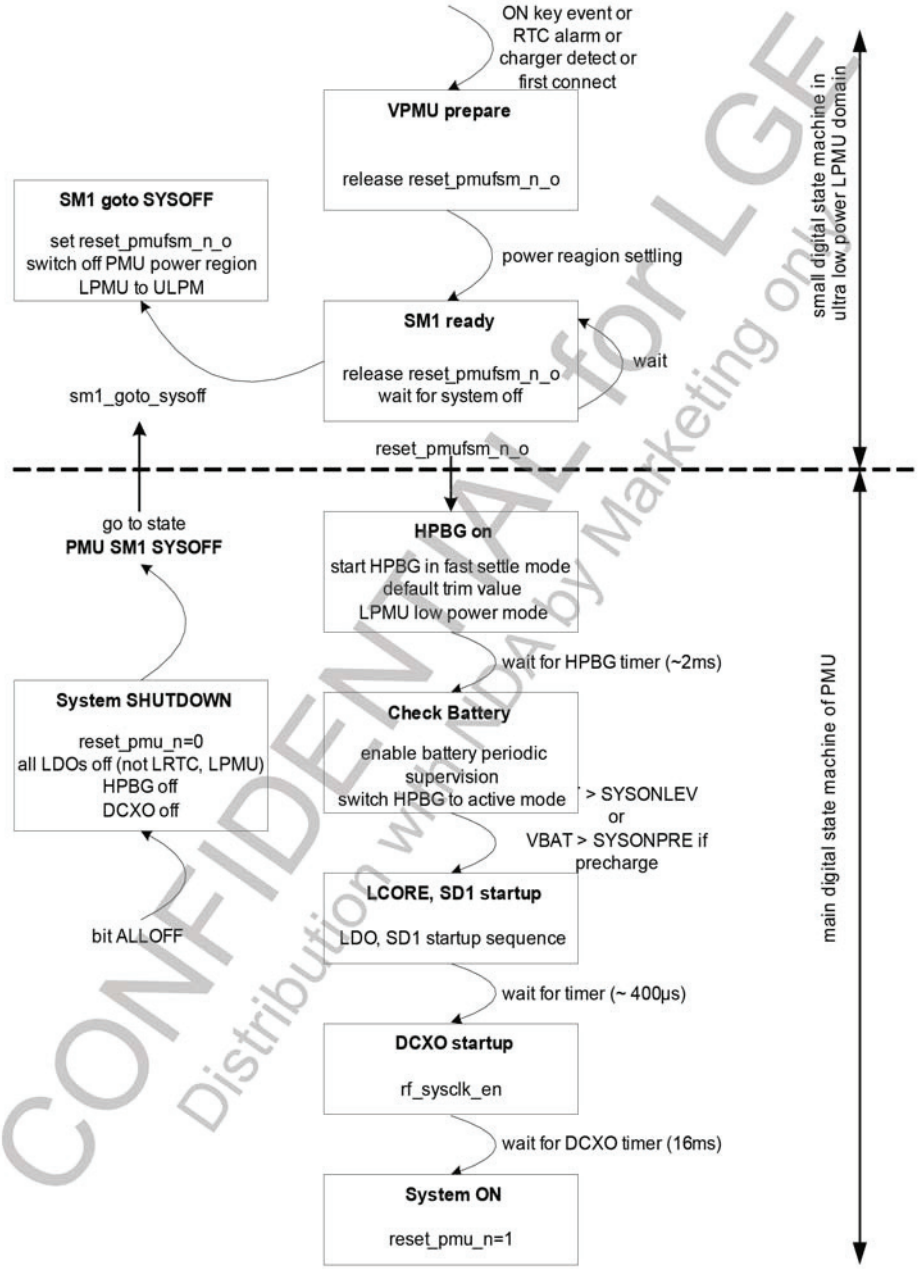


Figure 3.2.2 Second (Main) Part of the Startup State Machine in the VPMU Domain

3.2.2 Switching on due to first connect

If the battery voltage is connected the first time, that means the system enters the first time the SYSOFF state, this is stored in a first connect flag. If the first connect flag is set, the system will start immediately and not wait for any other system on event in the SYSOFF state.

3.2.3 Switching on due to on-Key event

The on key is connected to the ONKEY pad. The ESD protection and the input structure of this pad are connected to VRTC. If the ONKEY pad is forced to VRTC by an external key or similar circuit, the system starts. The ONKEY is sampled with the PMU clock. It has to be sampled four times high before a valid on event is generated. The status of the ON key can be read in the PMU registers, so it can be used as a functional key during phone operation also

3.2.4 Switching on due to RTC alarm

The real time clock can generate a wakeup signal called RTC alarm. This signal is sampled from the state-machine and after successfully detecting a high, the system is switched on.

3.2.5 Switching on due to charging

When a battery with a voltage below the SSONLEV level is inserted, the state machine will not start the system. As long as the battery voltage stays lover than SYSONLEV the system will stay off. The only possibility to start up the system is due to an external charger.

If an external charger is connected and detected and the battery is charged above the SYSONPRE voltage level the system will start up.
The PMU main state machine waits in the Check battery state until the battery voltage condition is fulfilled. The charger state machine provides the necessary pre-charge indication signal. This pre-charge signal is denounced in a small counter to have a stable signal. This is important, especially in half/full-wave charging where the charger detection is switching between charger detected/not detected according the AC supply frequency. Reasons for details on pre-charging see the charger chapter. The charger is controlled by an independent state machine. The pre-charge signal is used to trigger the pre-charge signal is used to trigger the pre-charge functionality. The charger state machine fully control the pre-charge, the PMU-state machine now changes to state HPBG on state and the system starts. This state change is indicated to the charger state-machine to enable the charger watchdog for safety.

3.2.6 Power Supply Start-up sequence

In order to avoid an excessive drop on the battery voltage caused by in-rush current during system power-on, possibly leading to system instability and “hick-ups” a staggered turn-on approach for the regulators is implemented. The regulators are turned on in a well defined sequence, thus spreading the in-rush current transients over time.

The IO’s of X-GOLD TM 213 are isolated in OFF mode (core supply is off). The isolation signal is controlled by the PMU state machine. This ensures that the PADs are in a well defined state during core supply settling. This allows to power up the LCORE core regulator and wait for the core to reach reset state before powering up the I/O supply regulators.

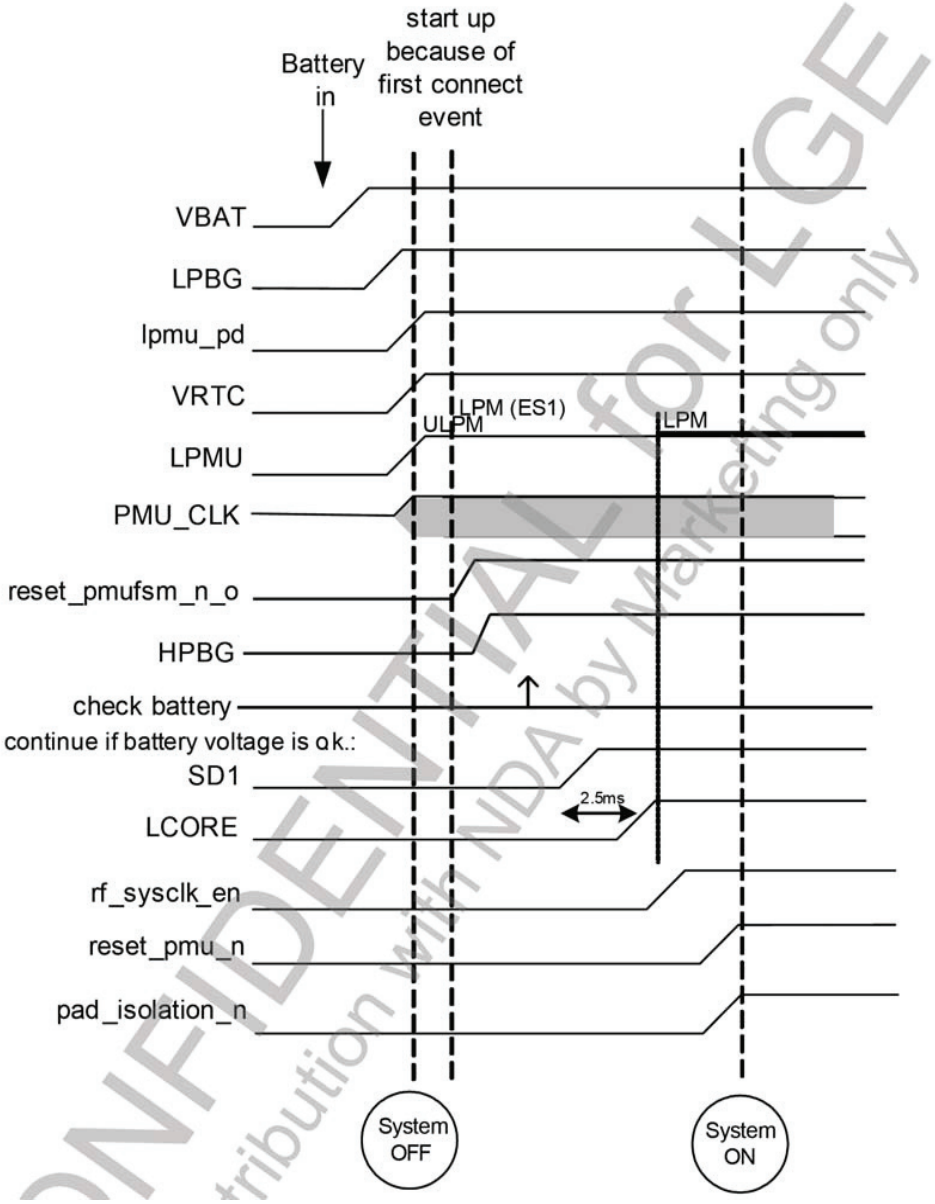


Figure 3.2.3 Start Up Sequence (triggered by First Connect Event)

3.2.7 External Reset Handling

The chip reset can be controlled by an external RESET_N ball. If this ball is pulled low, the chip will be reset. All PMU registers are reset during the external reset including LSIM control bits. The PMU statemachines are also not reset from the external reset. An SW or watchdog reset will not reset the PMU registers. A SW and Watchdog reset is seen on the reset_n pad to allow the reset of external devices. Basically there are three reset sources, first the reset signal controlled by the PMU (reset_pmu_n_o), second the reset signal controlled by the SCU (resetout_o) and third the external reset (RESET_N). The SCU reset is triggered by SW (for example due to a SW reset or watchdog reset). The PMU reset is controlled by the PMU state machine. The output of the reset handling block is the reset_postscu_n_o signal. This signal controls for example the µC subsystem and releases reset for the controller. During normal start up, the PMU releases the reset_pmu_n_o signal after entering the SYSTEM ON state. At this time the resetout_o signal is high, the RESET_N pad is not pulled low and therefore the reset_postscu_n_o signal follows the reset_pmu_n_o signal. That means the µC reset will be released and the µC starts operation. If the SW triggers an external reset via the SCU, signal resetout_o will be forced to low for a certain time and RESET_N will be forced to low by the open drain driver. At the same time the feedback to the SCU will be masked to not reset the baseband. The RESET_N pad is in the VDDRTC domain but the internal pull up is connected to the VDD_VDIG1 (1.8V) domain. That allows the pad to be used as reset for external devices running in the VDD1V8 domain. The RESET_N pad can also be used to monitor the chip internal reset condition during startup.

The open drain driver is a weak driver, that means it can be forced to high during debug from external pushing some current into the pad. In testmode signal reset_pmu_n_o is high, that means the chip reset is fully controlled from external.

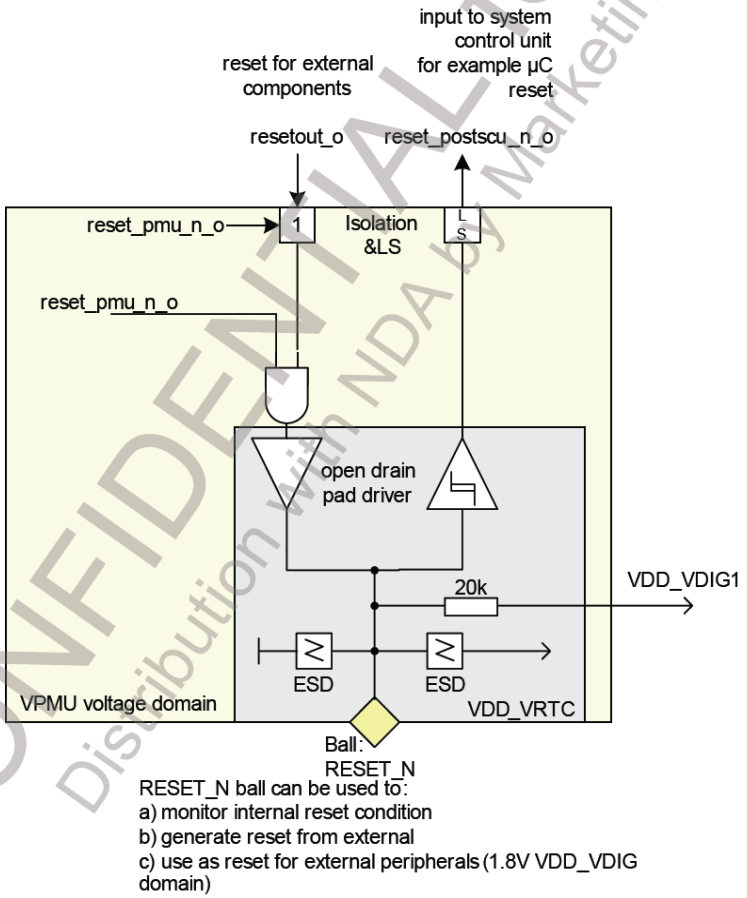


Figure 3.2.4 PMU, CGU and External Reset

3.2.8 Sysclock Switching

The PMU controls the rf_sysclk_en signal of the DCXO in the RF macro. During startup the PMU enables the DCXO. After the system is running the DCXO is controlled by the SCU of the baseband by using the vcxo_enable signal. This is handled by a dedicated logic in the PMU, see **Figure 21**. As long as rf_sysclk_en_pmu, the output of the PMU state-machine is high, vcxo_enable controls the rf_sysclk_en signal to the RF. If rf_sysclk_en_pmu is low, the DXCO is switched off, independent from vcxo_enable.

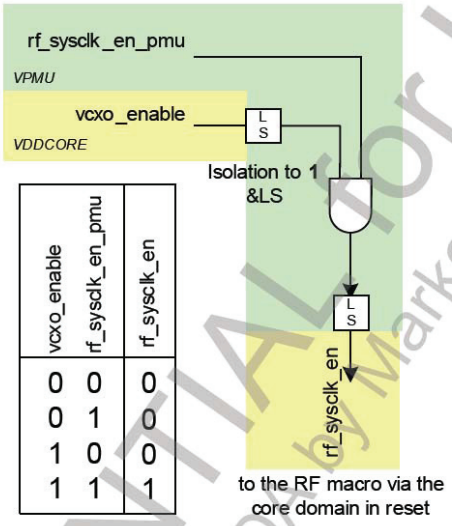


Figure 3.4.2 How sysclock Enable is Routed in the PMU

3.2.9 Undervoltage Shutdown

In active mode the PMU periodically measures the battery voltage using the ADC from the charger unit. If the battery is measured to be below the programmable shut-down level (called SYSOFF), the system changes to OFF mode. This is done via the SHUTDOWN state of the PMU state machine. (see chapter switch OFF)

3.2.10 Software Reset

A software reset does not affect any PMU register. The PMU register are reset with the reset_pmufsm_n_o signal. That means all PMU register are reset in OFF state. For details about the SW reset see chapter **External Reset Handling** .

3.2.11 PMU Clock

During the first startup (for example plugging in a battery) a PMU internal oscillator is used for generation of the PMU clock (pmu_clock). The frequency is slightly above 32 kHz (typ. 50 kHz) to be out of the audio band also for worst case devices. After first startup the software shall enable the 32 kHz crystal oscillator. It is not possible to use the 32 kHz oscillator during first startup, because the settling time of the oscillator can be quite long. After the 32 kHz oscillator is running and settled the software shall switch the PMU clock to the 32 kHz clock and disable the internal PMU oscillator for power saving reasons. The 32 kHz oscillator shall never be disabled after the PMU clock has been switched. The ADC in the charger unit has it's own oscillator generating a frequency of about 10 MHz. This oscillator is running during charging and during battery measurements triggered by the PMU. It is off otherwise.

3.2.12 System Sleep Mode

The sleep mode is controlled by using the VCXO_enable signal. This signal is used to switch the LDO's and the DC/DC converter SD1 in a programmable way into its low power mode (PFM). In addition DC/DC converter SD1 can be configured to change the output voltage to a lower value for additional power saving. VCXO_enable is also used to deactivate the HPBG and setting LDO LPMU in the ultra-low-power mode. In addition the DCXO is switched off by the VCXO_enable signal. The VCXO_enable signal is also used to switch some LDO's (software configured) to sleep and/or off mode or to change the output voltages of said LDO's. The state of the main PMU state machine is not changed due to VCXO_enable.

3.2.13 DC/DC Pre-Load Register Handling

The DC/DC converter works in different modes. If the mode is switched from PFM to PWM the pulse-width of the DC/DC converter depends on the current battery voltage (and on the output voltage). The PMU state-machine knows the battery voltage because of the battery supervision function. Depending on this value it selects a startup pulse-width for the DC/DC converter out of a register table. (4-values)

3.2.14 Power Down Sequence

Setting bit OFF in the GeneralControl register switches the system into OFF mode. After the turn off event, the state-machine switches to the SHUTDOWN state. The reset_pmu_n_o signal changes to low, the I/O pads are isolated using the padisolation_n signal, the LCORE LDO and the SD1 DC/DC converter are switched off, the LPMU LDO is switched to ultra-low power mode, the DCXO is turned off and the bandgap buffer is disabled. Before switching OFF the software shall have enabled the 32 kHz oscillator and has switched the PMU clock to the 32 kHz clock to archive the target OFF current.

3.3 FEM with integrated Power Amplifier Module (RF7161, U401)

3.3.1 Internal Block Diagram

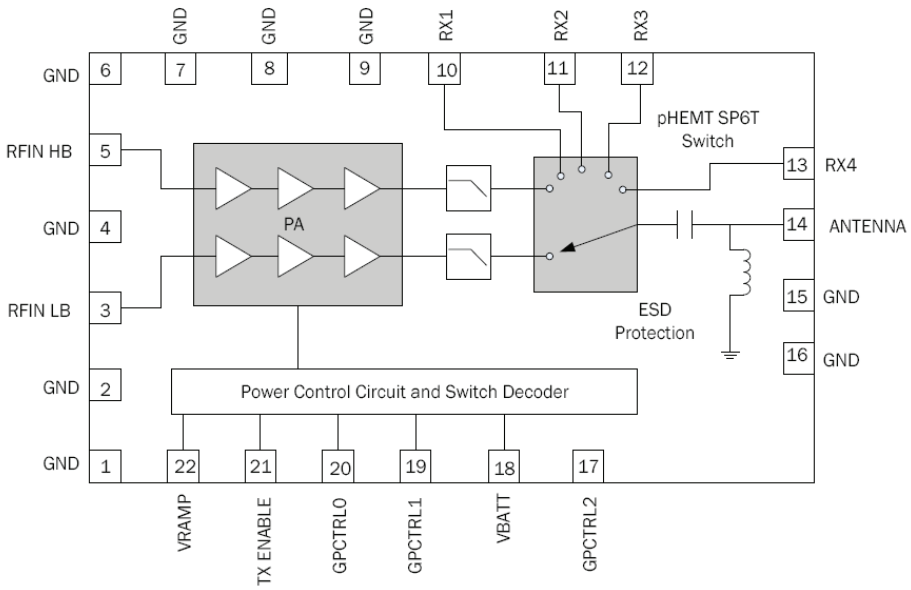


Figure. 3-3-1 RF7161 FUNCTIONAL BLOCK DIAGRAM

3.3.2 General Description

The RF7161 is a quad-band (GSM850/EGSM900/DCS1800/PCS1900) GSM/GPRS, Class 12 compliant transmit module with four interchangeable receive ports. This transmit module builds upon RFMD's leading power amplifier with PowerStar® integrated power control technology, pHEMT switch technology, and integrated transmit filtering for best-in-class harmonic performance.

The results are high performance, reduced solution size, and ease of implementation. The device is designed for use as the final portion of the transmitter section in a GSM850/EGSM900/DCS1800/PCS1900 handset and eliminates the need for a PA-to antenna switch module matching network.

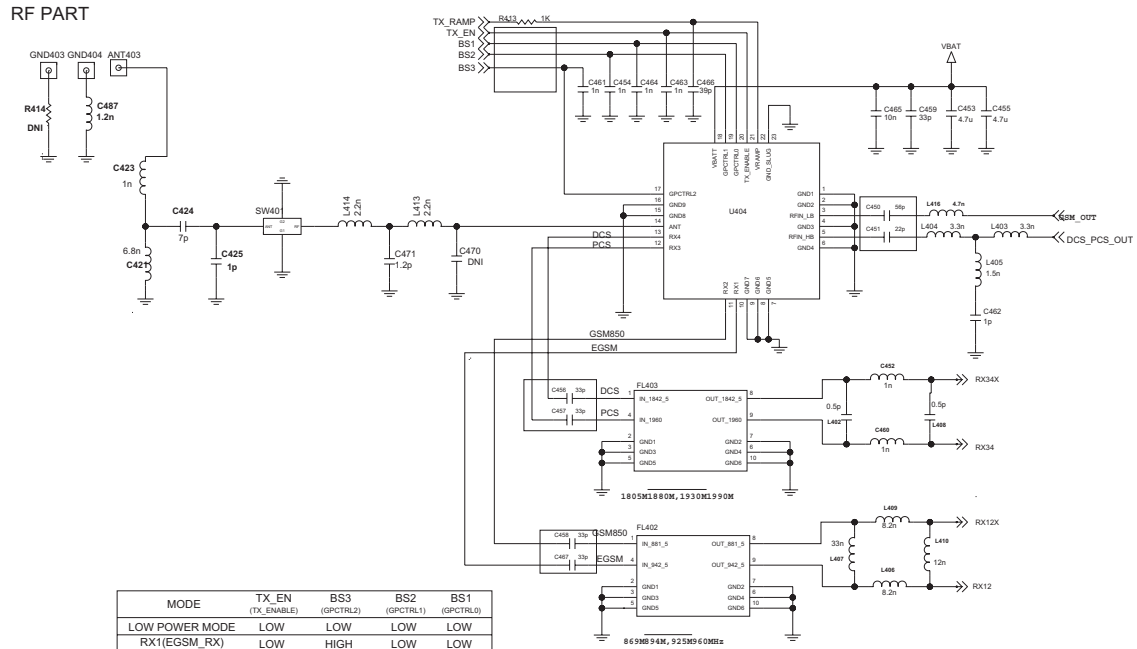
The RF7161 features RFMD's latest integrated power-flattening circuit which significantly reduces current and power variation into load mismatch. Additionally, a VBATT tracking feature is incorporated to maintain switching performance as supply voltage decreases.

The RF7161 also integrates an ESD filter to provide excellent ESD protection at the antenna port.
The RF7161 is designed to provide maximum efficiency at rated POUT.

MODE	TX_EN (TX_ENABLE)	BS3 (GPCTRL2)	BS2 (GPCTRL1)	BS1 (GPCTRL0)
LOW POWER MODE	LOW	LOW	LOW	LOW
RX1(EGSM_RX)	LOW	HIGH	LOW	LOW
RX2(GSM850_RX)	LOW	LOW	HIGH	LOW
RX3(PCS_RX)	LOW	LOW	HIGH	HIGH
RX4(DCS_RX)	LOW	LOW	LOW	HIGH
GSM850/900_TX	HIGH	LOW	HIGH	LOW
DCS/PCS_TX	HIGH	LOW	HIGH	HIGH

1. X = DON'T CARE
2. RX1, RX2, RX3, and RX4 are broadband receive ports and each supports the GSM850, GSM900, DCS, and PCS bands.

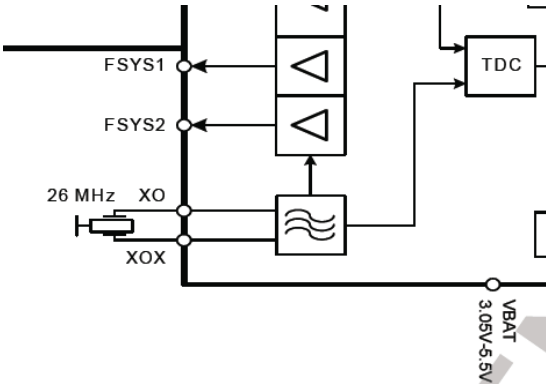
Figure 3.3.2 Band SW Logic Table



MODE	TX_EN (TX_ENABLE)	BS3 (GPCTRL2)	BS2 (GPCTRL1)	BS1 (GPCTRL0)
LOW POWER MODE	LOW	LOW	LOW	LOW
RX1(EGSM_RX)	LOW	HIGH	LOW	LOW
RX2(GSM850_RX)	LOW	LOW	HIGH	LOW
RX3(PCS_RX)	LOW	LOW	HIGH	HIGH
RX4(DCS_RX)	LOW	LOW	LOW	HIGH
GSM850/900_TX	HIGH	LOW	HIGH	LOW
DCS/PCS_TX	HIGH	LOW	HIGH	HIGH

Figure 3.3.3 FEM CIRCUIT DIAGRAM

3.4 Crystal(26 MHz, X100)



The X-GOLDTM213 RF-Subsystem contains a fully integrated 26 MHz digitally controlled crystal oscillator, designed for 8 pF crystals. The only external part of the oscillator is the crystal itself. Overall pulling range of the DCXO is approximately ±55 ppm, controllable by a 13-bit tuning word.

This frequency serves as comparison frequency within the RF-PLL and as clock frequency for the digital circuitry.
The 26 MHz reference clock can also be applied to external components like Bluetooth or GPS, via the two buffered output signals FSYS1 and FSYS2

Figure. 3.4.1 Crystal Oscillator External Connection

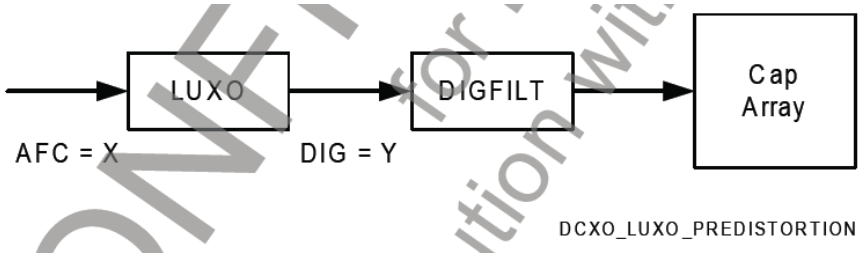


Figure. 3.4.2 Digital PREDISTORTION with LUXO

The DCXO tuning characteristic should be a first order linear function of the programming word AFC. The variable capacitance array is a first order linear function of the digital word DIG, which leads to a nonlinear curve ppm vs. DIG (and also a nonlinear ppm vs. AFC for DIG=AFC). In order to linearize the ppm vs. AFC curve the implementation of a predistortion is necessary.
To get the wanted linear ppm vs. AFC tuning curve some digital predistortion of the AFC word is required. This predistortion is performed by the linearization unit for crystal oscillator (LUXO). The LUXO calculates the corresponding DIG value according to the given AFC value.

3.5 RF Subsystem of PMB8810 (U102)

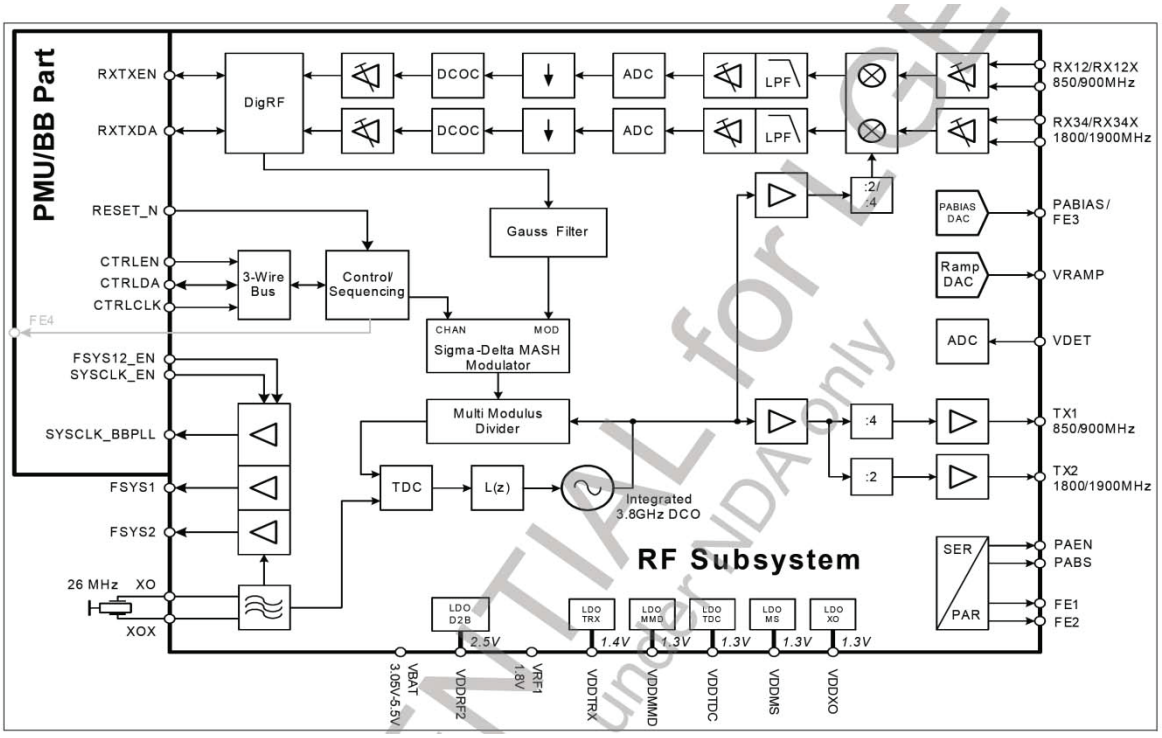


Figure. 3-5-1 Block DIAGRAM of RF Subsystem

3.5.1 GENERAL DESCRIPTION

The PMB8810 RF subsystem is designed for dual-band GSM voice and data applications (GPRS class 12). The system can be configured to support one low band, GSM850 or EGSM900, and one high band, DCS1800 or PCS1900. A block diagram of the RF subsystem is given in Figure 3-4-1.

3.5.2 FUNCTIONAL DESCRIPTION

3.5.2.1 Receiver

The X-GOLD™213 dual-band receiver is based on a Direct Conversion Receiver (DCR) architecture. Input impedance of the LNAs is optimized to achieve a matching without (external) high quality inductors. By use of frequency dividers (by 2/4) the LO frequency is derived from the RF frequency synthesizer.
The receive path is fully differential to suppress the on-chip interferences and reduce DC-offsets. The analog chain of the receiver contains two LNAs (low/high band), a quadrature mixer followed by an analog baseband filter and 14-bit continuous-time delta-sigma analog-to-digital converter. The filtered and digitized signal is fed into the digital signal processing chain, which provides decimation, DC offset removal and programmable gain control.

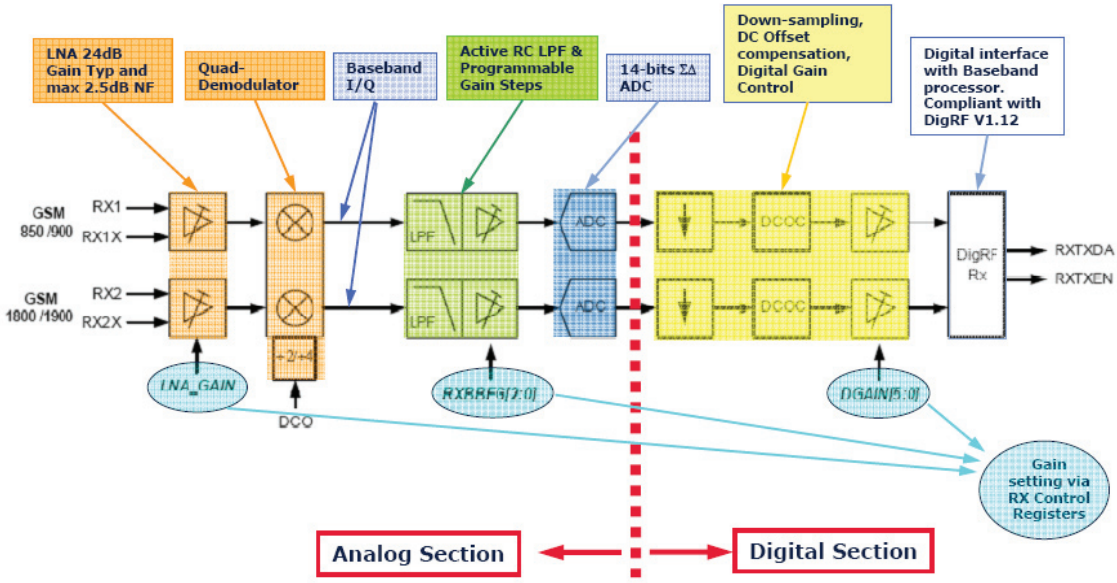


Figure. 3.5.2 RECEIVER CHAIN BLOCK DIAGRAM

3.5.2.2 Transmitter

The GMSK transmitter supports power class 4 for GSM850 or GSM900 as well as power class 1 for DCS1800 or PCS1900. The digital transmitter architecture is based on a fractional-N sigma-delta synthesizer for constant envelope GMSK modulation. This configuration allows a very low power design without any external components.
Up- and down-ramping is performed via the ramping DAC connected to VRAMP.

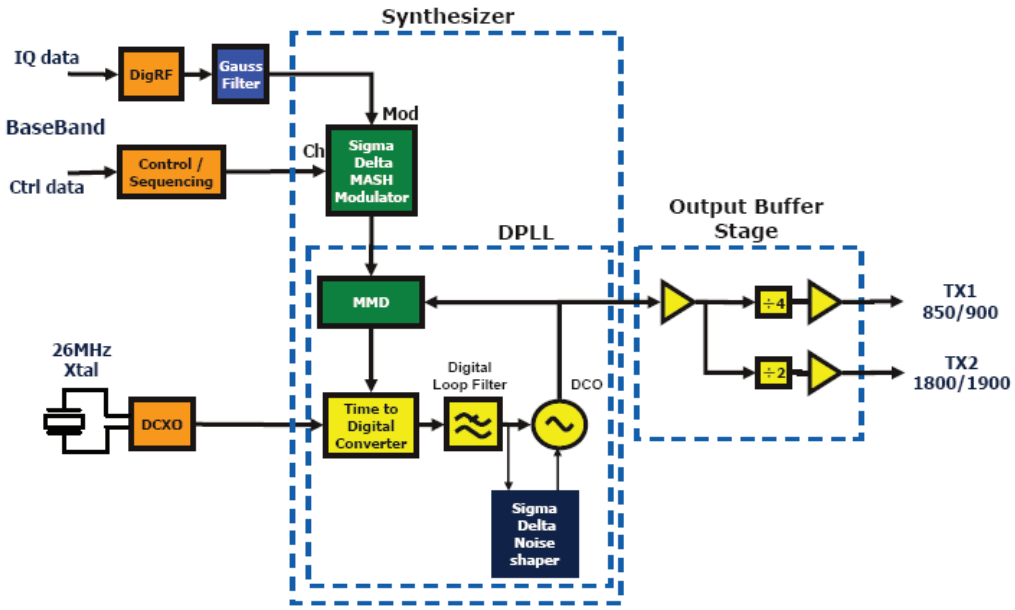


Figure. 3.5.3 TRANSMITTER CHAIN BLOCK DIAGRAM

RF synthesizer

The RF subsystem contains a fractional-N sigma-delta synthesizer for the frequency synthesis. Respective to the chosen band of operation the phase locked loop (PLL) operates at twice or forth of the target signal frequency. In receive operation mode the divided output signal of the digital controlled oscillator output (DCO) serves as local oscillator signal for the balanced mixer. For transmit operation the fractional-N sigma-delta synthesizer is used as modulation loop to process the phase/frequency signal. The 26 MHz reference signal of the phase detector incorporated in the PLL is provided by the reference oscillator.

3.5.2.3 Front-end/PA Control Interface

Two outputs (FE1, FE2) for direct control of antenna switch modules enable to select RX- and TX-mode as well as low- and high-band operation.
An extra band select signal PABS for the power amplifier is used, to support discrete PA and switching modules. Time accurate power dissipation of the PA is achieved by the control signal PAEN.
A minor set of power amplifiers require a bias voltage to enhance power efficiency. Support of this power amplifiers is achieved by the implemented bias DAC.

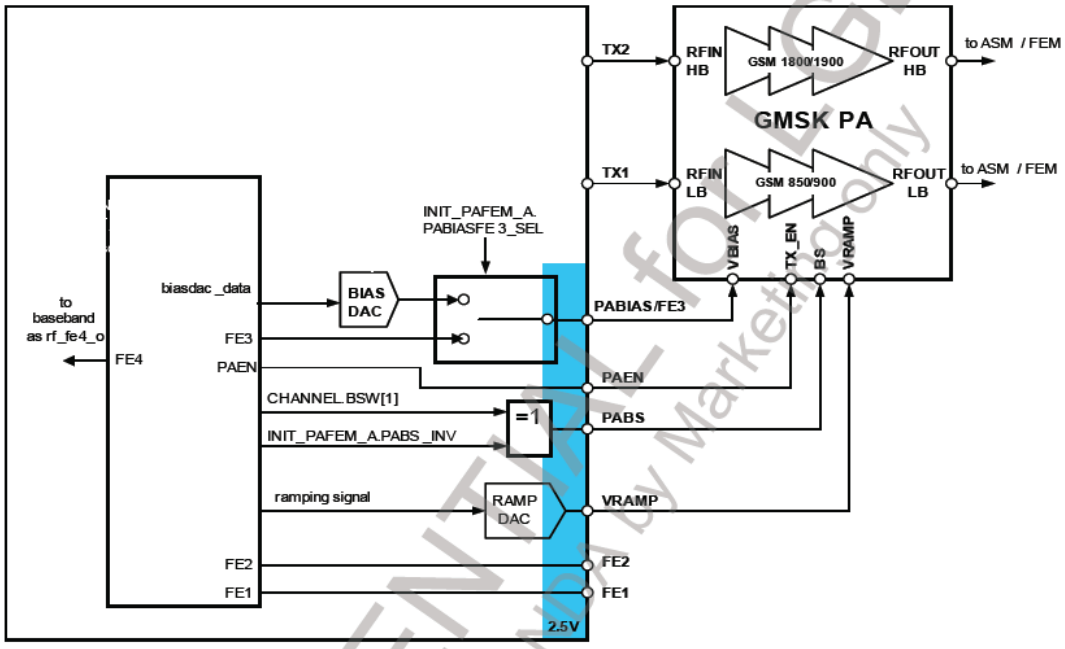


Figure. 3.5.4 PA AND FEM CONTROL BLOCK DIAGRAM

3.5.2.4 Power Supply

To increase power efficiency most parts of the RF subsystem are supplied by the DCDC converter situated in the PMU subsystem. Conversion of the 1.8 V output voltage of the DCDC to the 1.3 V/1,4 V circuit supply voltages is achieved by several Low-DropOut regulators (LDO).
One embedded direct-to-battery LDO provides the 2.5 V supply voltage for the remaining circuits.

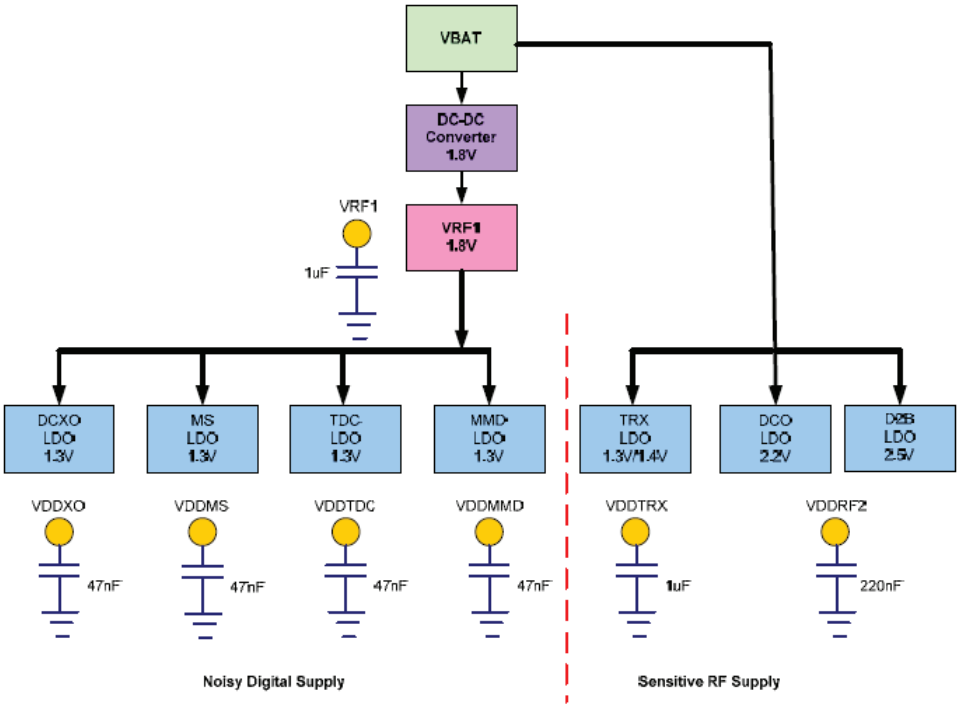


Figure. 3.5.5 POWER SUPPLY BLOCK DIAGRAM

3.6 MEMORY(PF38F5066M0Y3DE, U101)

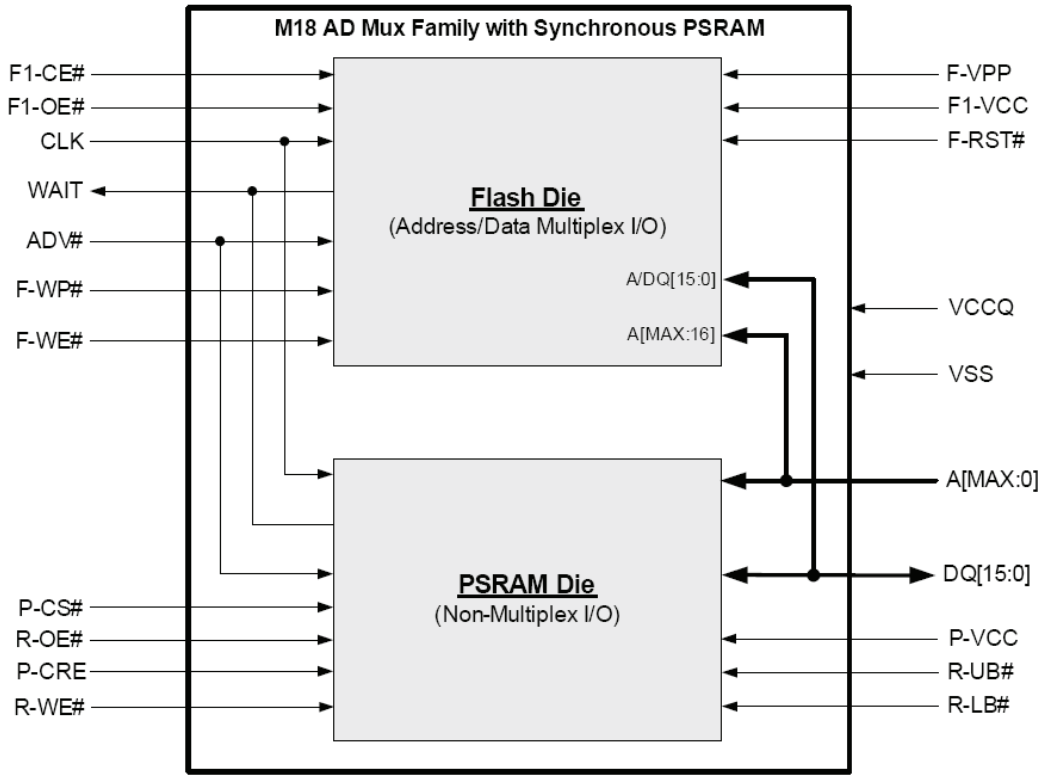


Figure. 3.6.1 MEMORY BLOCK DIAGRAM

The Numonyx™ StrataFlash® Cellular Memory (M18) device provides high read and write performance at low voltage on a 16-bit data bus.
The flash memory device has a multi-partition architecture with read-while-program and read-while-erase capability.
The device supports synchronous burst reads up to 108 MHz using ADV# and CLK address-latching (legacy-latching) on some litho/density combinations and up to 133 MHz using CLK address-latching only on some litho/density combinations. It is listed below in the following table.
.

Litho (nm)	Density (Mbit)	Supports frequency up to (MHz)	Sync read address-latching
90	256	133	CLK-latching
	512	108	Legacy-latching
65	128	133	CLK-latching
	256	133	CLK-latching
	512	108	Legacy-latching
	512	133	CLK-latching
	1024	108	Legacy-latching
	1024	133	CLK-latching

Table 3_6_1 M18 Frequency combinations

In continuous-burst mode, a data Read can traverse partition boundaries.

Upon initial power-up or return from reset, the device defaults to asynchronous arrayread mode. Synchronous burst-mode reads are enabled by programming the Read configuration Register. In synchronous burst mode, output data is synchronized with a user-supplied clock signal. A WAIT signal provides easy CPU-to-flash memory synchronization.

Designed for low-voltage applications, the device supports read operations with VCC at 1.8 V, and erase and program operations with VPP at 1.8 V or 9.0 V. VCC and VPP can be tied together for a simple, ultra-low power design. In addition to voltage flexibility, a dedicated VPP connection provides complete data protection when VPP is less than VPPLK.

A Status Register provides status and error conditions of erase and program operations.

One-Time-Programmable (OTP) registers allow unique flash device identification that can be used to increase flash content security. Also, the individual block-lock feature provides zero-latency block locking and unlocking to protect against unwanted program or erase of the array.

The flash memory device offers three power savings features:

• Automatic Power Savings (APS) mode: The device automatically enters APS following a read-cycle completion.

• Standby mode: Standby is initiated when the system deselects the device by deasserting CE#.

• Deep Power-Down (DPD) mode: DPD provides the lowest power consumption and is enabled by programming in the Enhanced Configuration Register. DPD is initiatied by asserting the DPD pin.

3.7 WiFi module

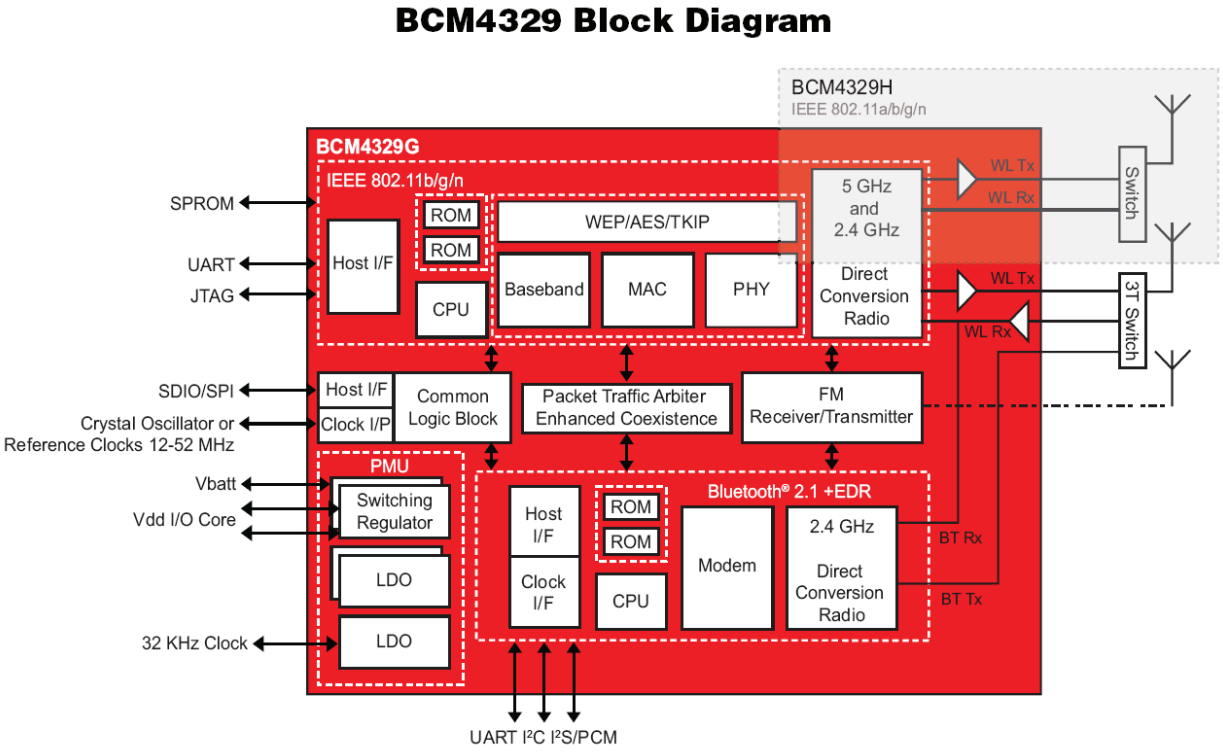


Figure 3_7_1. WiFi Module BLOCK DIAGRAM

The Broadcom® BCM4329 family of single chip devices provide the optimum integration of IEEE 802.11™ a/b/g and 802.11n (MAC/ baseband/radio) handheld device classes, Bluetooth® 2.1 + EDR (Enhanced Data Rate), and FM radio receiver and transmitter features in mobile and handheld wireless systems. The BCM4329 addresses the needs of compact mobile devices that require minimal power consumption. The BCM4329's integrated 2.4 GHz and 5 GHz WLAN CMOS power amplifiers offer the lowest cost dual-band solution in the industry. The BCM4329 utilizes advanced design techniques and process technologies to reduce active and idle power consumption and extend battery life, while maintaining robust connectivity and providing a rich set of features. The BCM4329's highly sophisticated InConcert radio coexistence algorithms and hardware mechanisms allow for an extremely collaborative coexistence scheme and provide coexistence support for a single shared antenna and external radios (including WiMax™ and cellular radio technologies). As a result, the BCM4329 enhances the overall quality of simultaneous voice, video, and data transmission of handheld systems, while minimizing the footprint. The BCM4329's integrated power management unit simplifies the power topology, enabling operation directly from the mobile's platform battery. Along with the integrated power amplifiers, the BCM4329 includes integrated transmit and receive baluns to further reduce overall cost.

3.7.1 Features

System Level Features • Industry's most integrated 65 nm single-chip combo device - Single-band (2.4 GHz) 802.11b/g/n or dual-band (2.4 GHz and 5 GHz) 802.11a/b/g/n with Bluetooth 2.1 + EDR and FM receiver and transmitter - Lowest overall cost solution • Full featured, on-chip Power Management Unit - Supports direct battery (2.3V to 5.5V) connection • Single driver software architecture for easy migration from existing to future embedded WLAN and Bluetooth devices • Integrates InConcert™ collaborative BT-WLAN coexistence with the industry's most robust coexistence performance - Supports IEEE 802.15.2 external three-wire coexistence scheme enabling support for additional wireless technologies like WiMax® • Shared Bluetooth and WLAN receive signal path (eliminates the need for an external power splitter while maintaining excellent sensitivity for both Bluetooth and WLAN)

• **Bluetooth and FM Key Features** • Bluetooth Core Specification Version 2.1 + EDR compliant with provisions supporting future specifications • Bluetooth Class 1 or Class 2 transmitter operation • Supports extended Synchronous Connections-Oriented (eSCO) transport for enhanced voice quality (by allowing retransmission of dropped packets) • Host Interface support - Host Controller Interface (HCI): High-speed UART - Audio: PCM - FM Control: HCI and BSC (I2C-compliant) ports - FM Audio: Stereo analog input and output, bidirectional I2S, and PCM ports • Increased battery life (reduced in power consumption in all operating modes) • FM receiver and transmitter (76 MHz to 108 MHz FM bands); Standards supported: - European Radio Data Systems (RDS) - North American Radio Broadcast Data System (RBDS) • Programmable FM transmit output power • Supports two simultaneous Advanced Audio Distribution Profiles (A2DP) for sharing music between two stereo Bluetooth headsets • Wideband speech support • Packet Loss Concealment (PLC) for improved RF link budget to headsets

WLAN Key Features • 802.11 a/b/g/n compliant • Supports a variety of 802.11n optional features such as Space Time Block Coding (STBC), Short Gual Interval (SGI), A-MPDU aggregation, Block Ack, Greenfield, RIFS • Industry-leading low-active transmit and receive power consumption and ultralow power in standby and idle modes • Supports IEEE 802.11d/e (WMM, QoS, WMM-PS), h, i, j (upgrades available for k, r, w) • Supports standard host interfaces SDIO v1.2 (50 MHz, 4-bit and 1-bit) and SPI (48 MHz) • Integrated CPU with on-chip memory for a complete WLAN subsystem (minimizes the need to wake up the applications processor) • Internal fractional nPL, allowing support for a wide range of reference clock frequencies • Security - WPA and WPA2 (personal) for powerful encryption and authentication - AES and TKIP in hardware for faster data encryption and 802.11i compatibility - Supports Cisco® Compatible Extensions (CCX - CCX4.0) - SecureEasySetup™ for simple Wi-Fi setup and WPA2/ WPA security configuration • Worldwide regulatory support (global products supported with worldwide homologated design) • Integrated power amplifier, baluns and LNA to meet the requirements of most handheld system (option to support external FEM)

3.8 SIM Card Interface

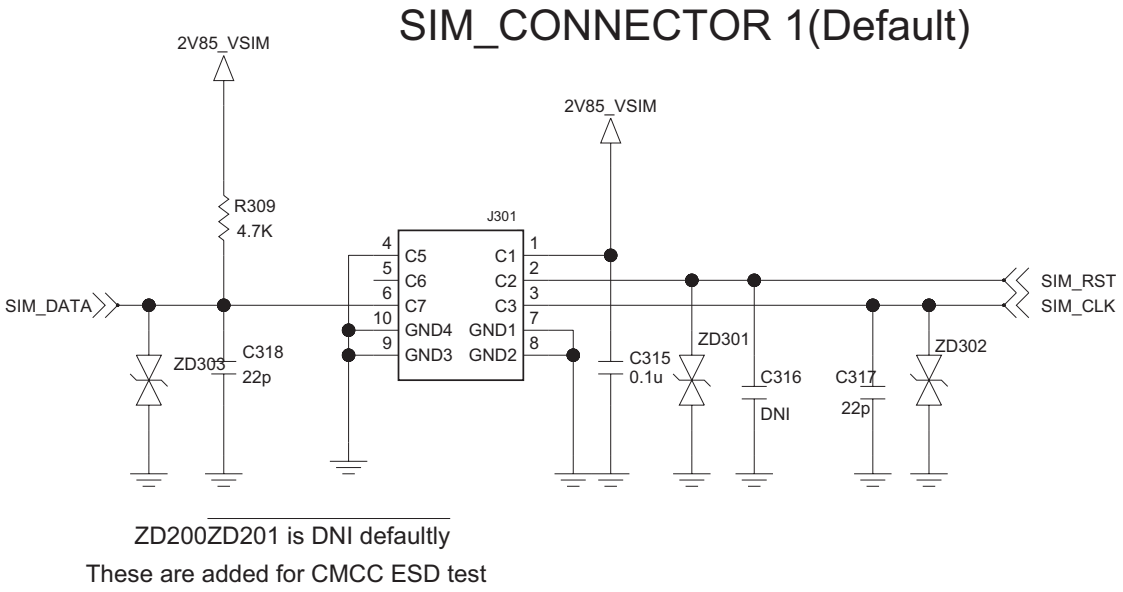


Figure 3-8-1. SIM CARD Interface

The Main Base Band Processor(XMM2130) provides SIM Interface Module.
The XMM2130 checks status Periodically During established call mode whether SIM card is inserted or not, but it doesn't check during deep sleep mode. In order to communicate with SIM card, 3 signals SIM_DATA, SIM_CLK, SIM_RST.
And This model supports 1.8/3V SIM Card.

Signal	Description
SIM_RST	This signal makes SIM card to HW default status.
SIM_CLK	This signal is transferred to SIM card.
SIM_DATA	This signal is interface datum.

3.9 LCD Interface

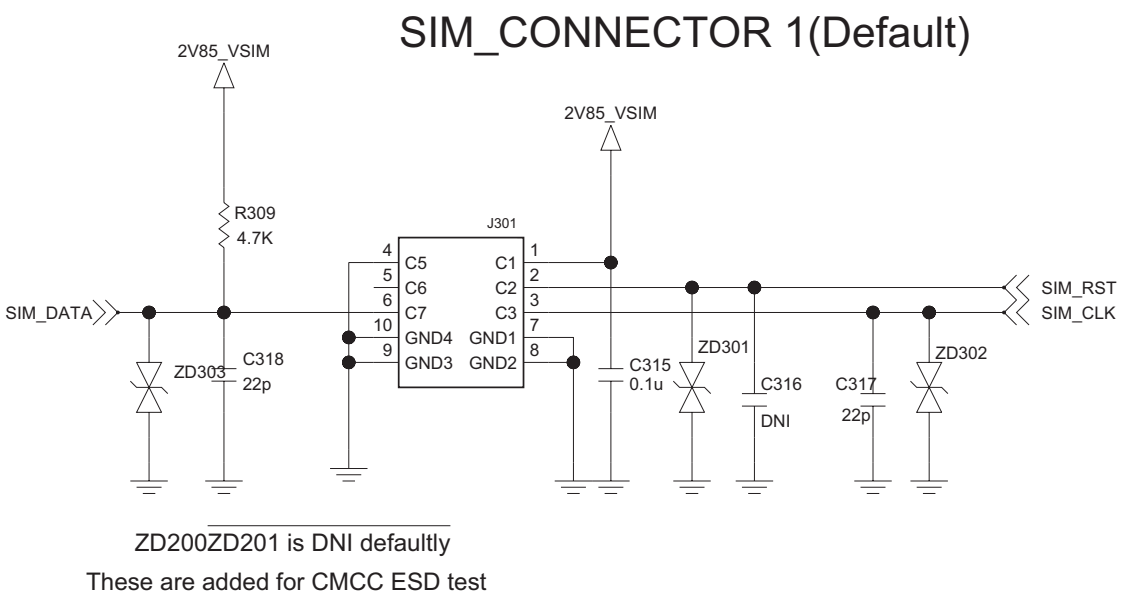


Figure 3-9-1. LCD Interface of LCD FPCB

The LS028Q3UW01 model is a Thin Film Transistor-Liquid Crystal Display without polarizer.

The matrix compose a-Si Thin Film Transistor as a active element.

It is a transmissive type display operating in the normally white mode. This TFT-LCD has 2.0 inch diagonally measured active display area with QVGA resolution (240xRGBx320 pixels) each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes. The LS028Q3UW01 has been designed to apply the interface method that enables low power.

The LS028Q3UW01 is intended to support applications where thin thickness, low power are critical factors and graphic display are important. In combination with the vertical arrangement of the sub-pixels, the LS028Q3UW01 characteristics provide an High quality display for mobile phone application.

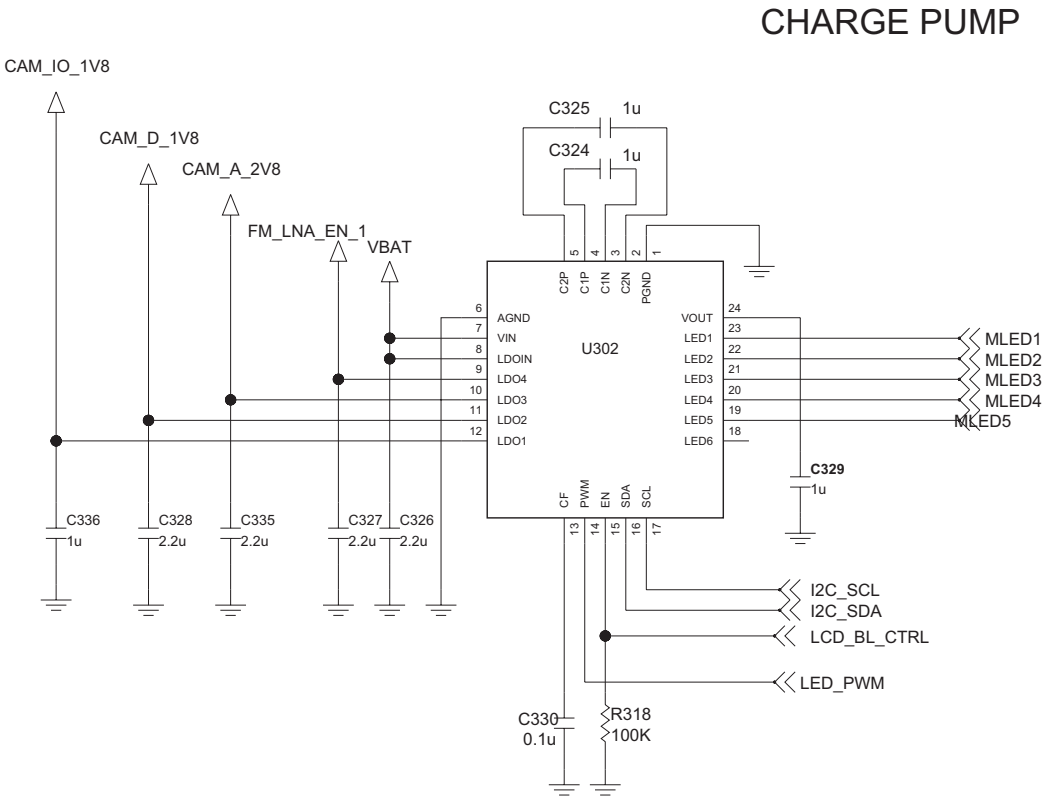


Figure 3-9-2. RT9396 CIRCUIT DIAGRAM

The RT9396 is a power management IC (PMIC) for backlighting and phone camera applications. The PMIC contains a 6-Channel charge pump white LED driver and four low dropout linear regulators.

The charge pump drives up to 6 white LEDs with regulated constant current for uniform intensity. Each channel (LED1 to LED6) supports up to 25mA of current. These 6-Channels can be also programmed as 4 plus 2-Channels or 5 plus 1-Channels with different current setting for auxiliary LED application.

The RT9396 maintains highest efficiency by utilizing a x1/ x1.5/ x2 fractional charge pump and low dropout current regulators. An internal 6-bit DAC is used for backlight brightness control. Users can easily configure up to 64-steps of LED current via the I2C interface control.

The RT9396 also comprises low noise, low dropout regulators, which provide up to 200mA of current for each of the four channels. The four LDOs deliver 3% output accuracy and low dropout voltage of 200mV @ 200mA.

Users can easily configure LDO output voltage via the I2C interface control. The LDOs also provide current limiting and over-temperature functions. The RT9396 is available in a WQFN-24L 3x3 package.

LED Backlight Current

RT9396 communicates with a host (master) Using the standard I2C 2-wire interface.

The two bus lines of SCL and SDA must be pulled high when the bus is not in use. Internal pull-up resistors are installed. After the START condition, the I2C master sends a chip address. This address is eight bits long, consisting of seven address bits and a following data direction bit (R/W). The RT9396 address is 10101000 (A8h) and is a receive-only (slave) device. The second word selects the register to which the data will be written. The third word contains data to write to the selected register. Figure 2 shows the writing information for the four LDOs as well as for each LED current. In the second word, the sub-address of the four LDOs is "001" and the sub-address of the LED Driver for different dimming modes are respectively "010", "011" and "100". For the LDO output voltage setting, bits B1 to B4 represent each LDO channel respectively where a "1" indicates selected and a "0" means not selected. The B0 bit controls on/off (1/0) mode for the selected LDO channel(s). Then, in the third word, bite C0 to C3 control a 16-step setting of LDO1 to LDO4.The voltage values are listed in Table 1. For LED dimming, there are three operating modes (Backlight I, Backlight II and Backlight III) to select from by writing respectively "010", "011" and "100" into the First three bits of the second word, It should be noticed that no matter which mode is selected, LED1 to LED3 must be turned on, else LED4 to LED6 can not be Turned on. When backlight I is selected, all six LEDs have the same behavior. Their 64-step dimming currents are set by bits C0 to C5, which are listed in Table 2. The bits C6 and C7 determine the fade in/out time of each step as shown in Figure 2. For Backlight II and Backlight III, two sets of LEDs, called Main and Sub, can work separately.

Backlight Quiescent Current

The quiescent current required to operate all four backlights is reduced by 1.5mA when backlight current is set to 4.0mA or less. This feature results in higher efficiency under light-load conditions. Further reduction in quiescent current will result from using fewer than four LEDs.

3.10 Battery Charger Interface

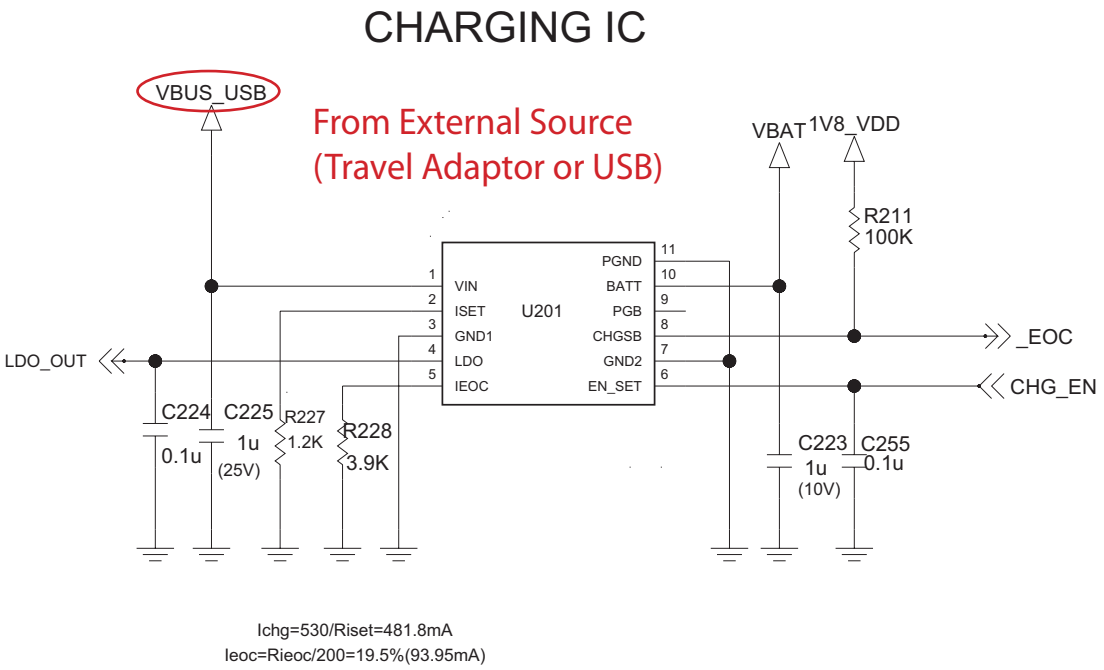


Figure 3-10-1 BATTERY CHARGER BLOCK

The RT9524 linear battery chargers safely charges single-cell Li+ batteries.
Charging rate is optimized to accommodate the thermal characteristics of a given application.
There is no need to reduce the maximum charge current or worst-case charger power dissipation.
Charging is optimized for Li+ cells using a control algorithm that includes low-battery precharging, voltage and current-limited fast charging, and top-off charging, while continuously monitoring for input overvoltage and device over-temperature.
The charge current and termination threshold are programming by simple one wire serial interfaces.
The charger status is indicated by two open-drain outputs.

The AC adapter charger current is programming by external ISET1 resistor while USB charge current is programming either 90mA or 400mA through one wire interface.

The RT9524 is available in the tiny 10pin 2mm by 3mm TDFN package.

3.11 Keypad Interface

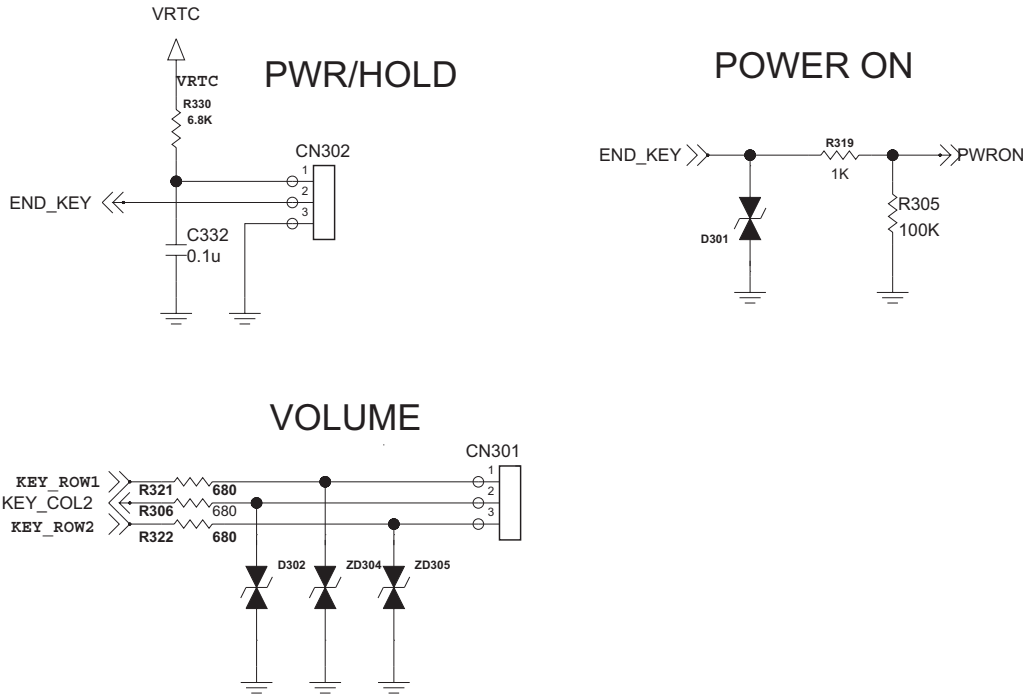


Figure 3-11-1 MAIN KEY STRUCTURE

The Keypad Interface is a peripheral controller, which can be used for scanning external keypad matrices with up to 8 rows and 8 columns (that is 64 standard keys). By adding an additional row of keys connected to ground the number of keys can be extended by up to 8 keys. This results in a maximum number of 72 keys to by identified by the Keypad Interface Controller.
The Keypad Scan Module reduces the number of interrupts and polling through the processor and therefore reduces the power consumption. The module is able to debounce and scan the external keypad matrix automatically without any software intervention. After debouncing it generates an interrupt. The interface controller contains information about the key (or key combination) that was pressed and how long it was pressed.

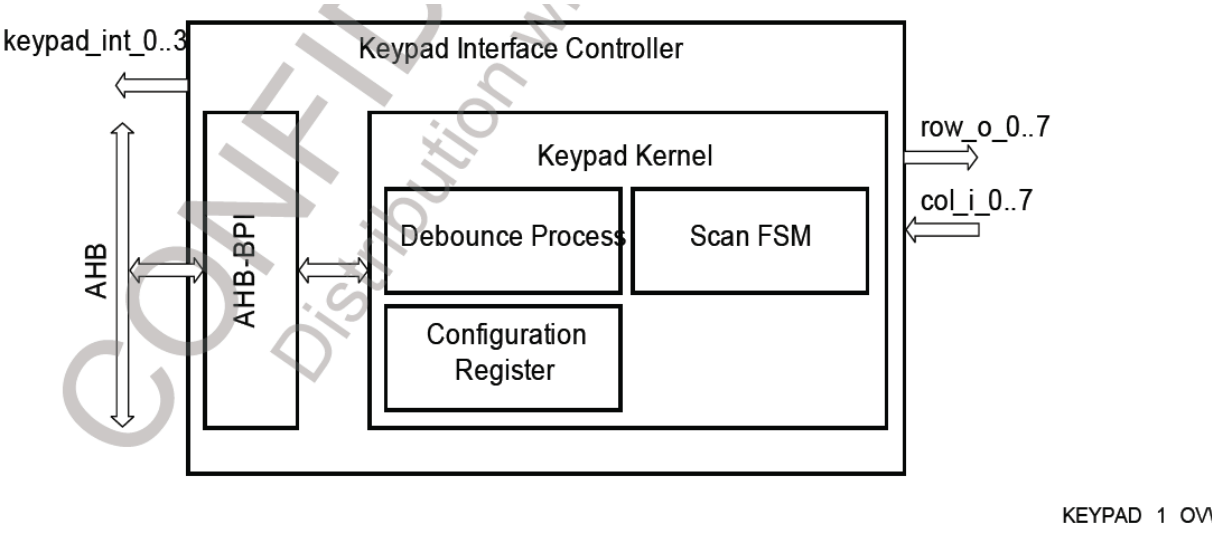


Figure 3-11-3 Block Diagram and System Integration of the KPD

3.12 Audio Interface

3.12.1 Functional Overview

The audio front-end of X-GOLD™213 offers the digital and analog circuit blocks for both receive and transmit audio operation, from a mobile phone perspective (called audio-in and audio-out subsequently). It features a high-quality, stereo digital-to-analog path with amplifier stages for connecting acoustic transducers to X-GOLD™213. In audio-in path the supply voltage generation for electret microphones, a low-noise amplifier and analog to digital conversion are integrated in X-GOLD™213. A more detailed functional description will be given in the following sections.

The audio front-end itself can be considered to be organized in three sub-blocks:
- Interface to processor cores (TEAKLite® and - indirectly - ARM)
- Digital filters
- Analog part

The following figure shows an architecture overview of the Audio section.

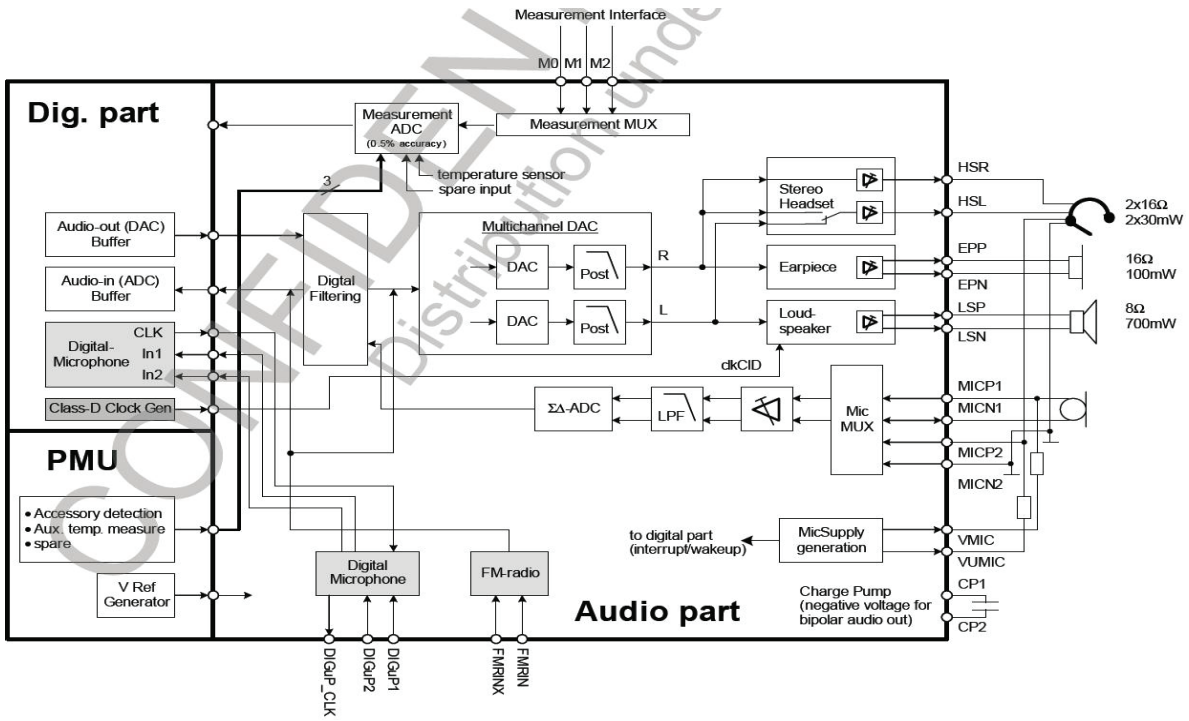


Figure 3.12.1 Audio Section Overview

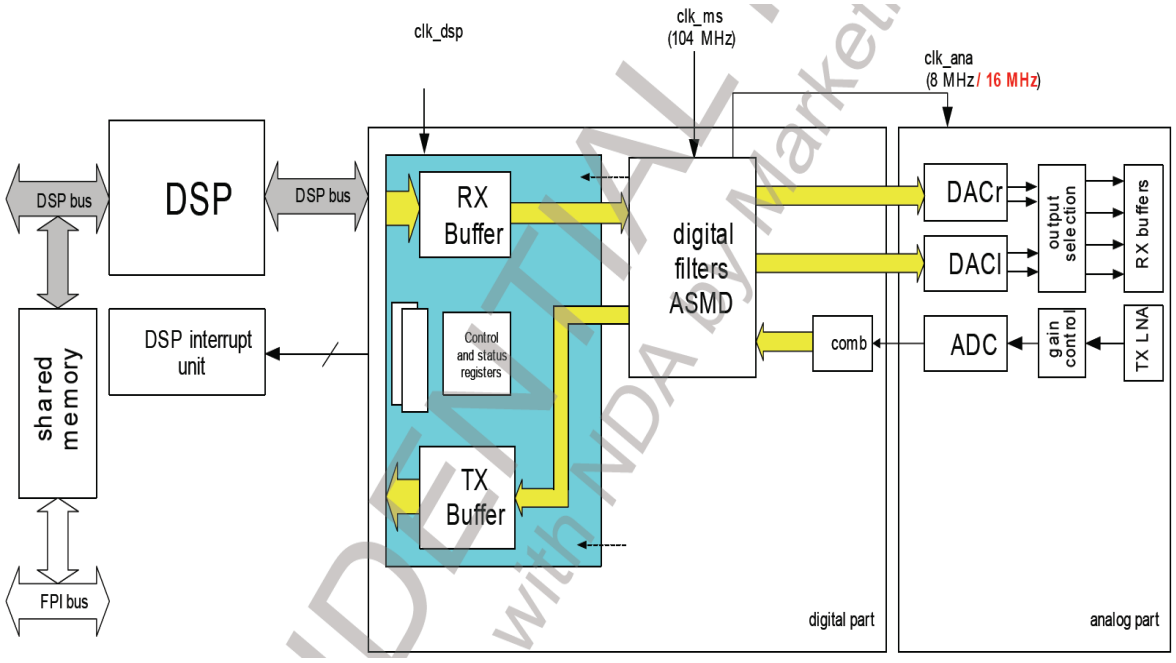


Figure 3.12.2 Overview of Clocking and Interfaces of Audio Front End

The audio front-end of X-GOLD™213 has the following major operation modes:

• Power-down: All analog parts are in power down and all clocks of the digital part are switched off.
• Audio mode: Digital decimation/interpolation filters are connected to the interface buffers and the analog part is enabled.

These major modes can be modified by certain control register settings.
• Due to the new gain settings in the TX path, the maximum input voltage is limited to 0.8 Vpp.
• In both voiceband paths, the value range for voice samples is confined to 97.5%, i.e. to [-31948, 31947] or [8334H, 7CCBH] in X-GOLD™213.
• On the TX path, 83% "1"s on the VTPDM line correspond to a 16-bit value of 7CCBH and 17% "1"s correspond to a 16-bit value of 8334H at the digital filter output. Thus the usable range is 66%. This range can be scaled to 100% by Firmware.
• The high-pass functions of the voiceband filters have to be implemented in firmware on TEAKLite®.

3.12.2 Digital Part

The digital part of the X-GOLD™213 audio front-end comprises an interface to the TEAKLite® bus, interfaces to the interrupt units of TEAKLite®, digital interpolation filters for oversampling digital-to-analog conversion, digital decimation filters for analog-to-digital conversion and an interface to the analog part of the audio front-end. For the digital microphone all the filtering is done in a dedicated hardware. The output sample stream is then fed in a duplicated ring buffer structure like the data from the analog microphone path (after A/D conversion and subsequent digital filtering).

▪ Interpolation Filter
The interpolation path of the X-GOLD™213 audio front-end increases the sampling rate of the audio samples to the rate of the digital-to-analog converter. Because the input sampling rates can vary between 8 kHz and 47.619 kHz the filter characteristic and oversampling ratio can be adjusted to the respective sampling rate. The requirements for the interpolation filters depend on the sampling rate, because a sufficient out-of-band discrimination in the audio frequency band (20 Hz,...,20 kHz) has to be ensured.

▪ Decimation Filter
The digital decimation filter on X-GOLD™213 has two operating modes: 8 kHz output sampling rate and 16 kHz output sampling rate (or 16 kHz output sample rate and 16kHz bandwidth in case of doubled ASMD clock).

3.12.3 Analog Part

The analog part of the X-GOLD™213 audio front-end in audio-out direction consists of a stereo digital to analog converter (multi-bit oversampling converter) which transforms the output of the digital interpolation filter into analog signals. It is followed by the gain control/amplifier section. The DAC outputs can be switched to several output buffers. In audio-in section there is an input multiplexer which selects either one of two differential microphone inputs to be connected to the low-noise amplifier and analog pre-filter. The signals from the analog pre-filter are input to a second-order sigma-delta analog-to-digital converter. In addition there is a connection for FM-radio playing.

▪ Audio-out Part
The analog audio-out part consists of two multi-bit digital-to-analogue converters (DAC) and an output stage. The signal sources are switched to the output drivers in the output stage. The output drivers consist of: a) one mono, differential class-D Loudspeaker driver, b) one mono, differential Earpiece driver and c) one stereo, single-ended (with uni- or bipolar signals), Headset driver.

▪ **Digital-to-analog converters**
The multi-bit oversampling DACs of the X-GOLD™213 audio front-end convert the 16-bit data words coming from the digital interpolation filters to analogue signals.

▪ **Output Amplifier**
The different output buffers in X-GOLD™213 are driven by the outputs of the selection block. The differential earpiece driver can be used to drive a 16 Ω earpiece and works in differential. The two single ended headset drivers can be used to drive a 16 Ω headset. They can work unipolar mode, where an AC coupling of the headset might be needed, or can work also in bipolor mode. The differential loudspeaker driver can be used to drive a 8 Ω loudspeaker. As it is a class-D amplifier the needed suppression of the higher harmonics of the switching signals
has to be achieved by the external circuitry. The buffers are designed to be short circuit protected.

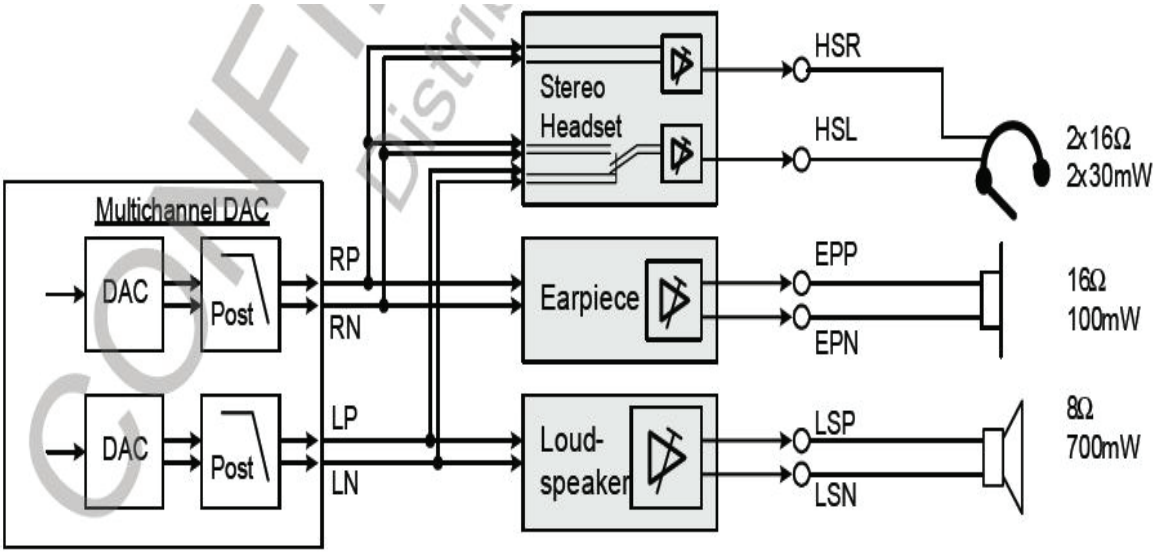


Figure 3.12.3 Switching for R/L DACs onto Buffers

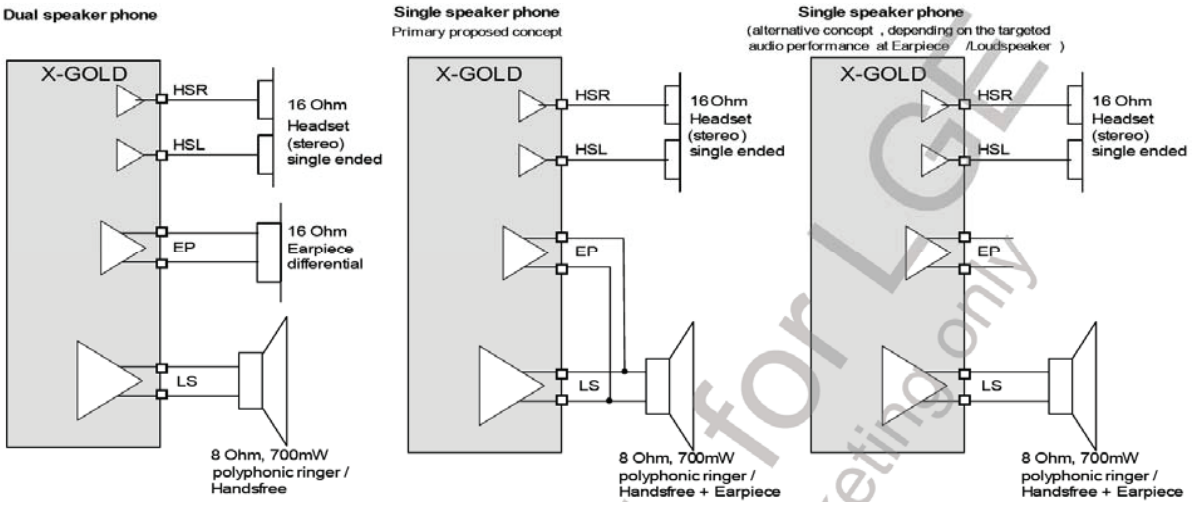


Figure 3.12.4 Different Application Scenarios

In order to achieve the single-speaker concept by parallel connection of Earpiece and Headset amplifier the Earpiece amplifier have to sustain the up to 5 V voltage of the class-D amplifier.

▪ Audio-in Path

The audio-in path of X-GOLD™213 provides two differential microphone input sources, MIC1and MIC2.

• The inputs for microphone MIC1 are MICP1 and MICN1.
• The inputs for microphone MIC2 are MICP2 and MICN2.

The audio-in path consists of an input selector, a low noise amplifier and following pre-filter with gain control, a second order ΣΔ-converter and a digital decimation filter. It supports both standard GSM (bandwidth 3.5 kHz) and wideband (bandwidth 7 kHz) speech bands.
The differential input signal from the microphone first passes a low noise amplifier and following pre-filter and an anti-aliasing pre-filtering stage achieving and overall variable gain ranging from 0 dB to +39 dB . The signal is then modulated by a second order ΣΔ-converter which is clocked with the same clock rate as the digital to analog converters. The ΣΔ-converter delivers a 1-bit pulse density modulated data stream at a rate of 2 MHz to the digital decimation filter which reduces the rate to 8 kHz or 16 kHz, depending on the current mode.
To improve SNR the sample frequency can be doubled in dedicated modes and the modulated data stream is 4MHz instead of 2 MHz.

▪ Microphone Supply

X-GOLD™213 has a single ended power-supply concept for electret microphones:
For both modes a minimal load capacitance of t.b.d. nF is necessary to guarantee stable operation of the buffer.
The maximal load capacitance must not exceed t.b.d. nF.
2 microphone supplies VMIC and VUMIC are available. The supply VUMIC has a ultra-low-power mode, where the current consumption is minimum, whilst at the same time the noise performance is reduced.
For this purpose the VUMIC is directly supplied out of the VMIC regulator, the Mic-Buffer can be switched off and only the quiescent current of the VMIC regulator is present. This mode can be used to supply a headset and allow accessory detection with highly reduced current consumption For normal operation the supply can be switched to normal operation mode with improved noise performance. In case of an digital microphone VMIC can be used for supplying this microphone.

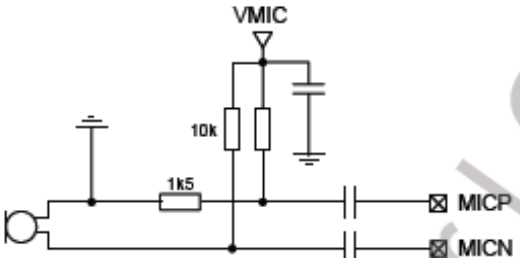


Figure 3.12.5 Typical Microphone Supply Generation (alternative)

3.13 Camera Interface(2M Fixed Focus Camera)

3.13.1 PMB8810 Camera Interface

The Camera Interface (CIF) represents a complete video and still picture input interface (see Figure 26).

The CIF contains image processing, scaling, and compression functions. The integrated image processing unit supports image sensors with integrated YC_bC_r processing.
Scaling is used for downsizing the sensor data for either displaying them on the LCD, or for generating data streams for MPEG-4 compression. In general, YC_bC_r 4:2:2 JPEG compressed images should use the full sensor resolution, but they can also be downscaled to a lower resolution for smaller JPEG files. Scaling also can be used for digital zoom effects, because the scalers are capable of up-scaling as well.
CIF all data is transmitted via the memory interface to an AHB bus system using a bus master interface. Programming is done by register read/write transactions using an AHB slave interface.

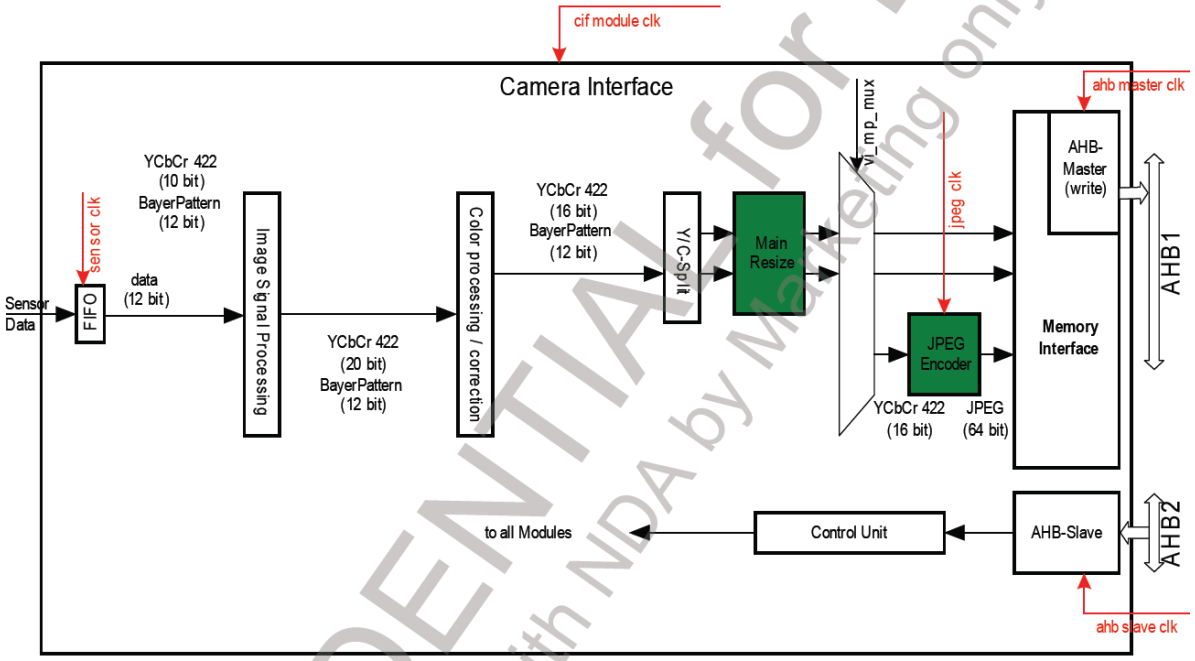


Figure 3.13.1 Block Diagram of Camera Interface

Functional Overview of CIF

The following list gives an overview over the CIF's functionality:

- 78 MHz system clock
- 78 MHz sensor clock
- 78 MHz JPEG encoder clock
- 32-bit AHB slave programming interface
- ITU-R BT 601 compliant video interface supporting YC_bC_r
- ITU-R BT 656 compliant video interface supporting YC_bC_r data
- 8-bit camera interface
- 12-bit resolution per color component internally
- YC_bC_r 4:2:2 processing
- Hardware JPEG encoder incl. JFIF1.02 stream generator and programmable quantization and Huffman tables
- Windowing and frame synchronization
- Continuous resize support
- Frame skip support for video (e.g. MPEG-4) encoding
- Macro block line, frame end, capture error, data loss interrupts and sync. (h_start, v_start) interrupts
- Programmable polarity for synchronization signals
- Luminance/chrominance and chrominance blue/red swapping for YUV input signals
- Maximum input resolution of 3 Mpixels (2048x1536 pixels)
- Main scaler with pixel-accurate up- and down-scaling to any resolution between 3 MP (2048x1536) and 32x16
- pixel in processing mode
- Buffer in system memory organized as ring-buffer
- Buffer overflow protection for raw data and JPEG files
- Asynchronous reset input, software reset for the entire IP and separate software resets for all sub-modules
- Interconnect test support
- Semi planar storage format
- Color processing (contrast, saturation, brightness, hue)
- Power management by software controlled clock disabling of currently not needed sub-modules

3.14 Touch Interface

The touch controller is an analog interface circuit for a human interface touch screen device.

All of touch functions are composed of a register-based architecture and are controlled through the internal register sets by serial interface.

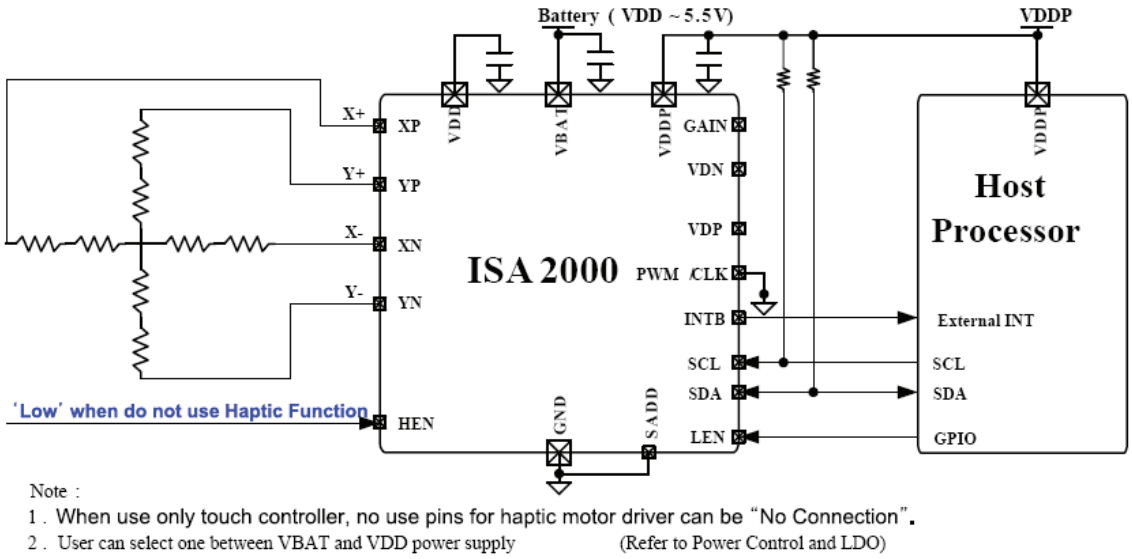


Figure 3-14 Touch Driver Block Diagram

• Operation

As the ISA2000 is a slave device, controls and communication with the ISA2000 is done via a serial interface under control of the host processor. The touch controller is operated by two operating mode with selectable, one is the single operating mode and another is the automation operating mode. During operates as single operating mode, control of the ISA2000 and its functions is accomplished by writing simple write and read commands of serial interface for getting the selected input ADC conversion, so user can get the each data among X-position, Y-position and Z-position of ADC conversion per serial interface write and read commands After receiving INTB signal. While, during operates as automation operating mode, user can get all of X-position, Y- position and Zposition of ADC conversion per serial interface write and read commands after finishing the all of ADC conversion.

3.15 Vibrator Interface

The haptic motor driver is a single chip supply haptic driver for improved sensory experience in mobile phone and other handheld devices. This function is capable of driving up to 250mA at 3V supply voltage and has overcurrent limitation function. Near rail-to-rail output swing under load ensures sufficient voltage drive for most ERM (Eccentric Rotating Mass)/LRA (Linear Resonant Actuator) type actuators, while the differential output drive allows the voltage polarity across the actuator to be reversed quickly. Reversing the voltage gives the haptic motor driver the ability to drive an actuator both clock-wise and counter clock-wise.

These features fast turn on time, and a wide input voltage range for precise speed control. A low power shutdown mode minimizes power consumption.

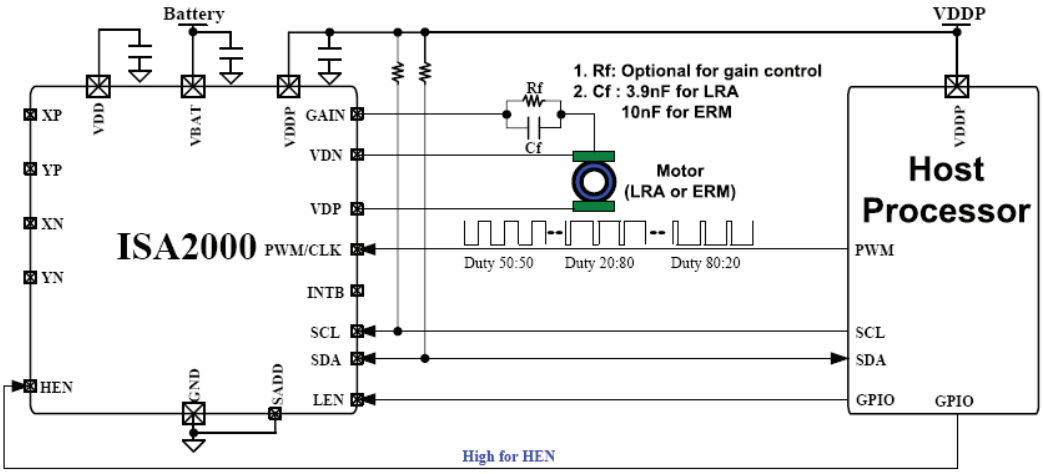
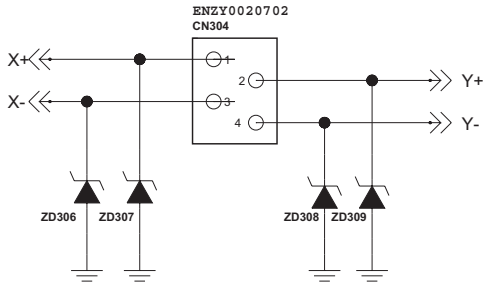


Figure 3-15-1 Vibrator Driver Block Diagram

TOUCH CONNECTOR



Touch & Haptic Driver Ckts

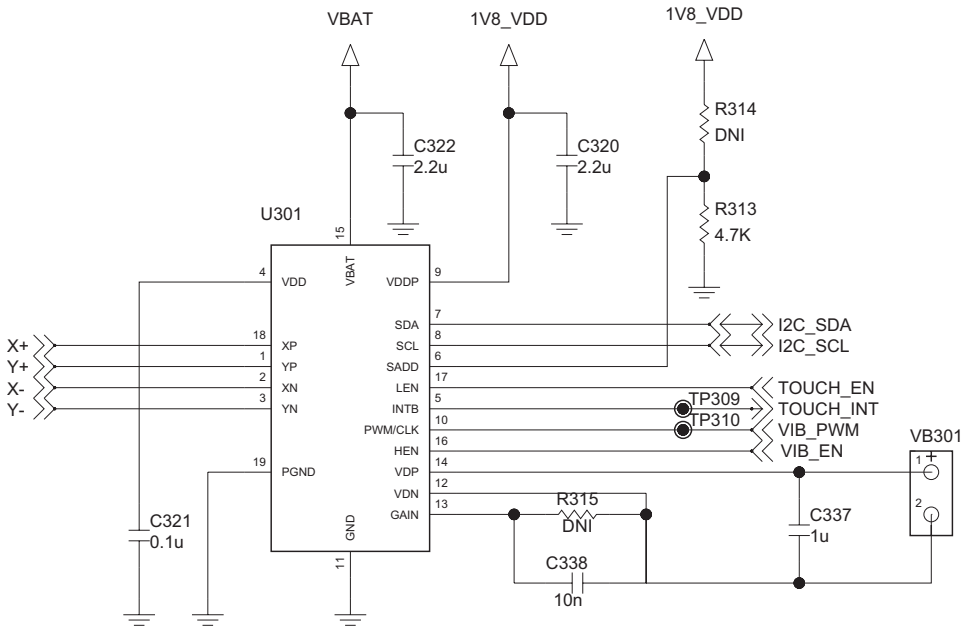


Figure 3-15-2 Touch &Vibrator Driver Block

4. TROUBLE SHOOTING

4.1 RF Component

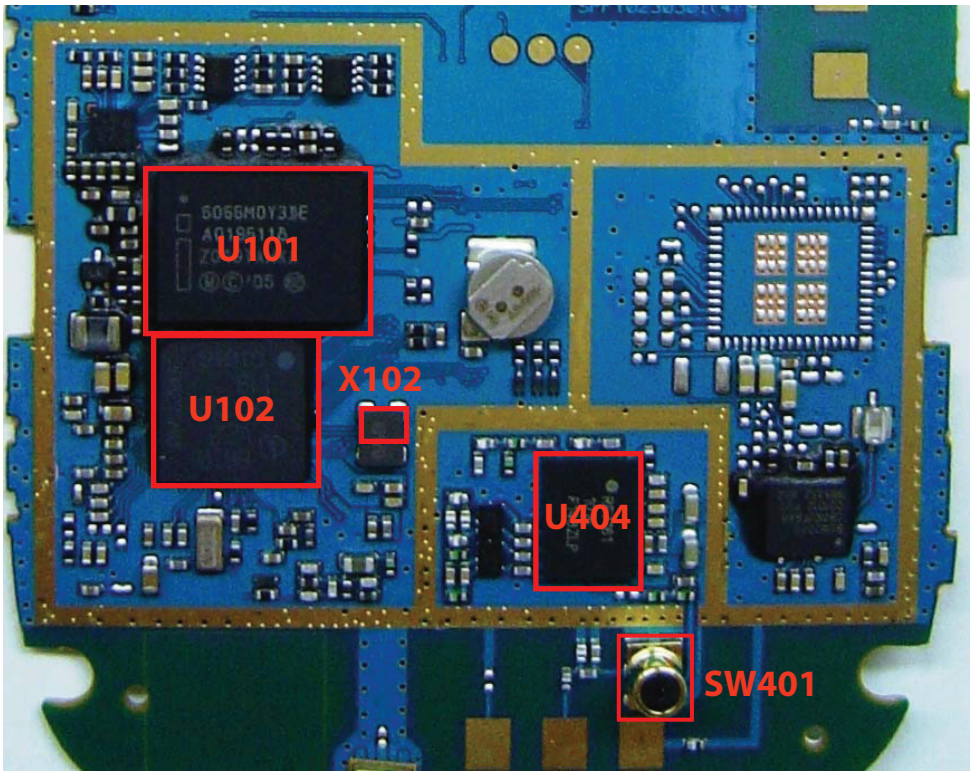
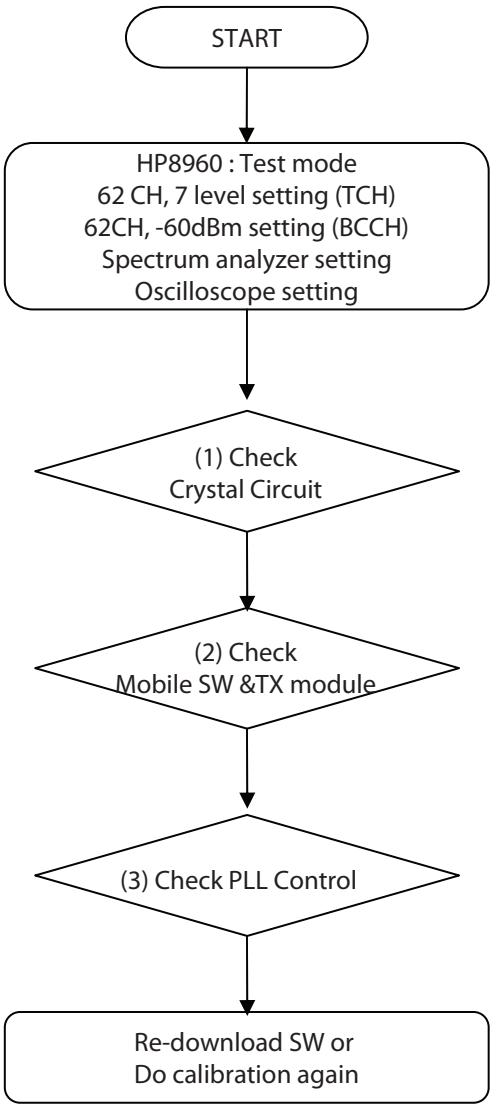


Figure 4.1

U101	Memory(1G NOR/256pSRAM) PF38F6066M0Y3DE
U102	Main Chip (A-GOLDRADIO) PMB8810(XMM213)
U404	GPRS QUAD TX MODULE RF7161
X102	Crystal, 26MHz Clock DSX321G-26M(8PF)
SW401	RF Switch NMS-306(RF500)

4.2 RX Trouble

CHECKING FLOW



(1) Checking Crystal Circuit

TEST POINT

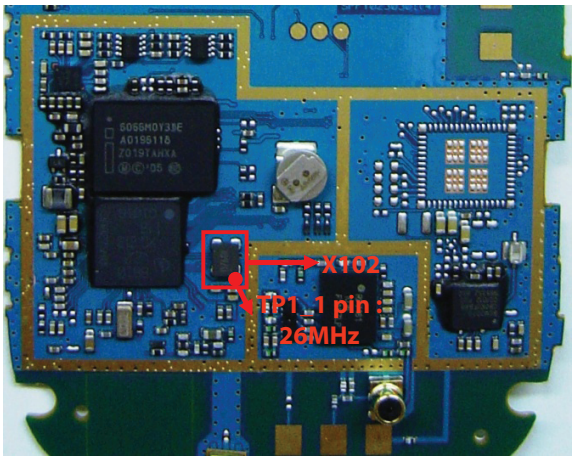
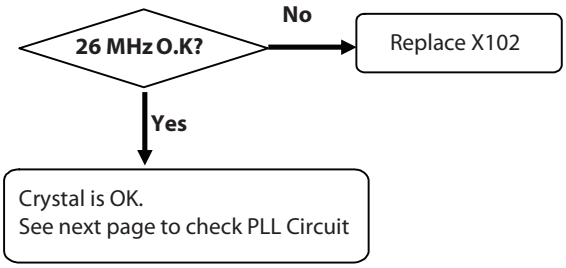


Figure 4.2.1

CHECKING FLOW



CIRCUIT

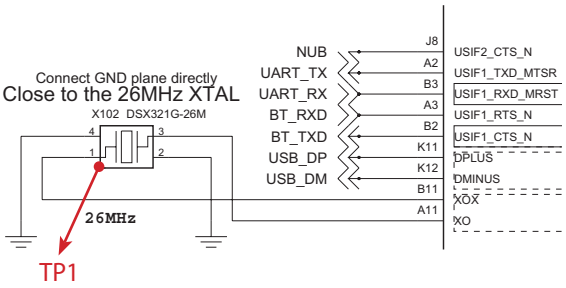


Figure 4.2.2

WAVEFORM

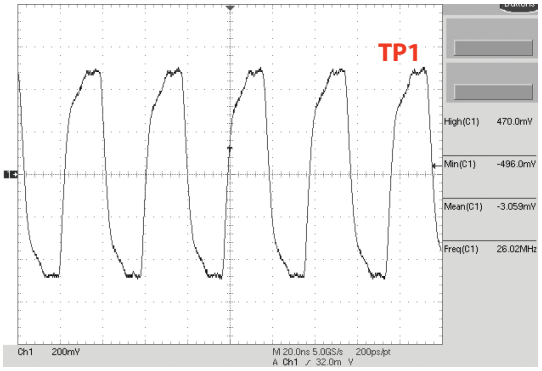


Figure 4.2.3

(2) Checking Mobile SW &TX Module

TEST POINT

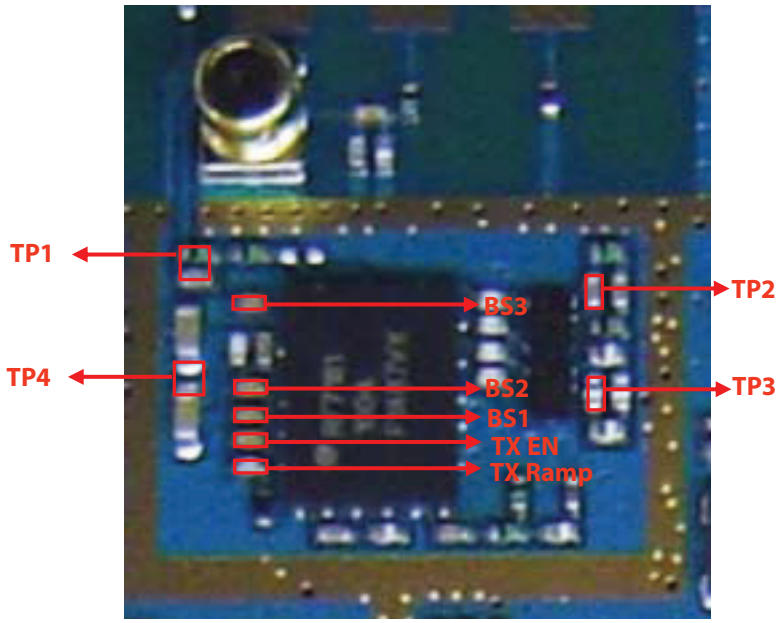
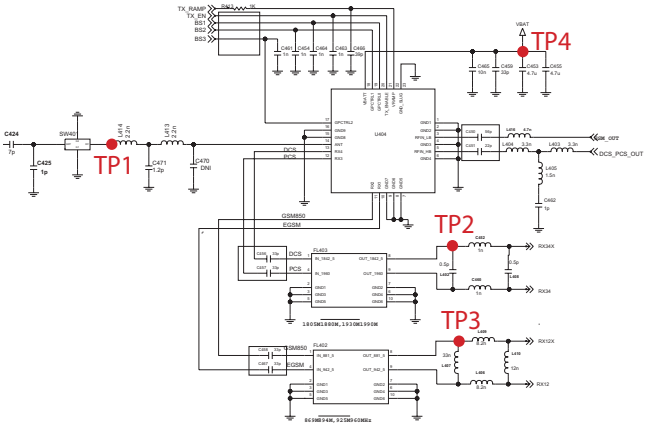


Figure 4.2.4

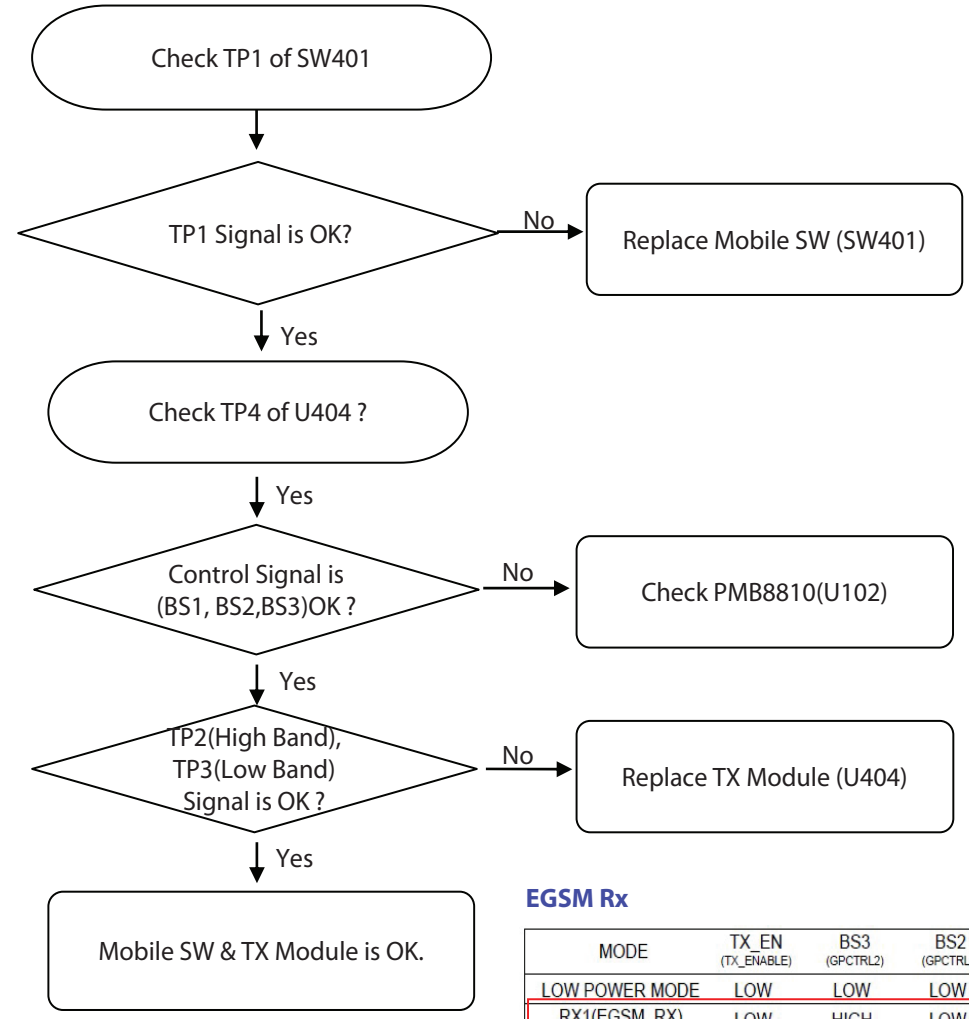
CIRCUIT



CONTROL LOGIC

EGSM Rx

CHECKING FLOW

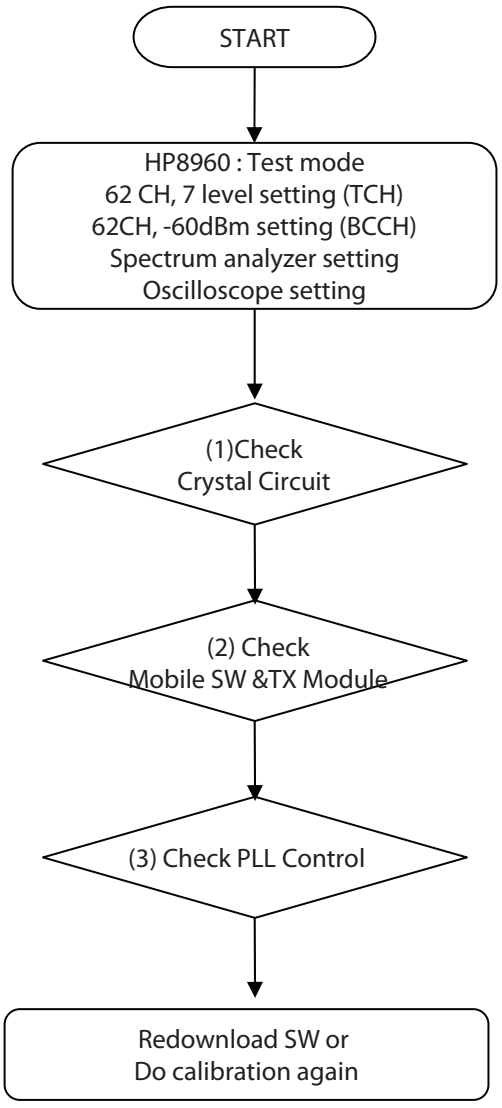


EGSM Rx

MODE	TX_EN (TX_ENABLE)	BS3 (GPCTRL2)	BS2 (GPCTRL1)	BS1 (GPCTRL0)
LOW POWER MODE	LOW	LOW	LOW	LOW
RX1(EGSM_RX)	LOW	HIGH	LOW	LOW
RX2(GSM850_RX)	LOW	LOW	HIGH	LOW
RX3(PCS_RX)	LOW	LOW	HIGH	HIGH
RX4(DCS_RX)	LOW	LOW	LOW	HIGH
GSM850/900_TX	HIGH	LOW	HIGH	LOW
DCS/PCS_TX	HIGH	LOW	HIGH	HIGH

4.3 TX Trouble

CHECKING FLOW



(1) Checking Crystal Circuit

TEST POINT

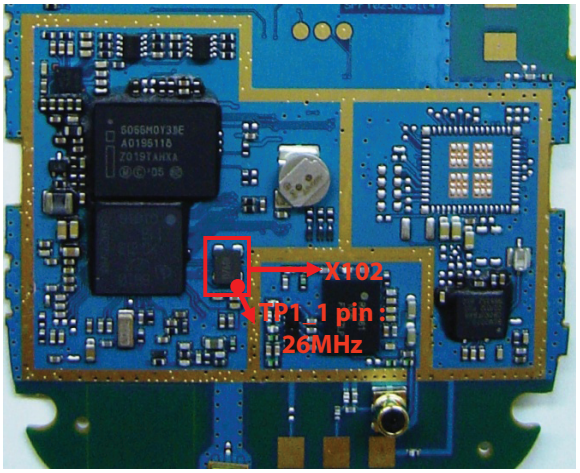
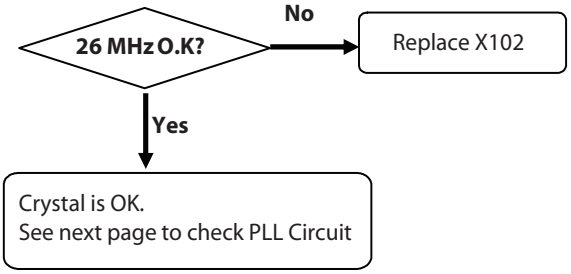


Figure 4.3.1

CHECKING FLOW



CIRCUIT

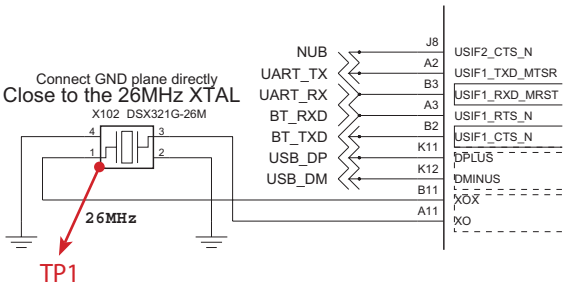


Figure 4.3.2

WAVEFORM

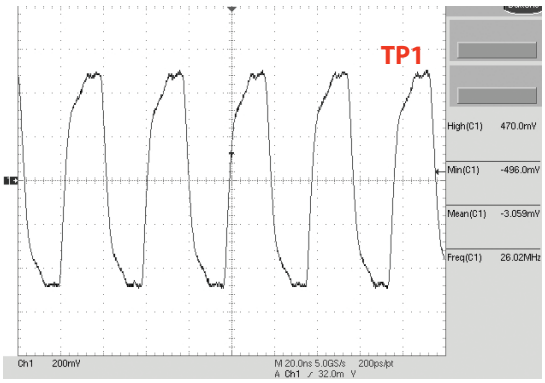


Figure 4.3.3

(2) Checking Mobile SW & TX Module

TEST POINT

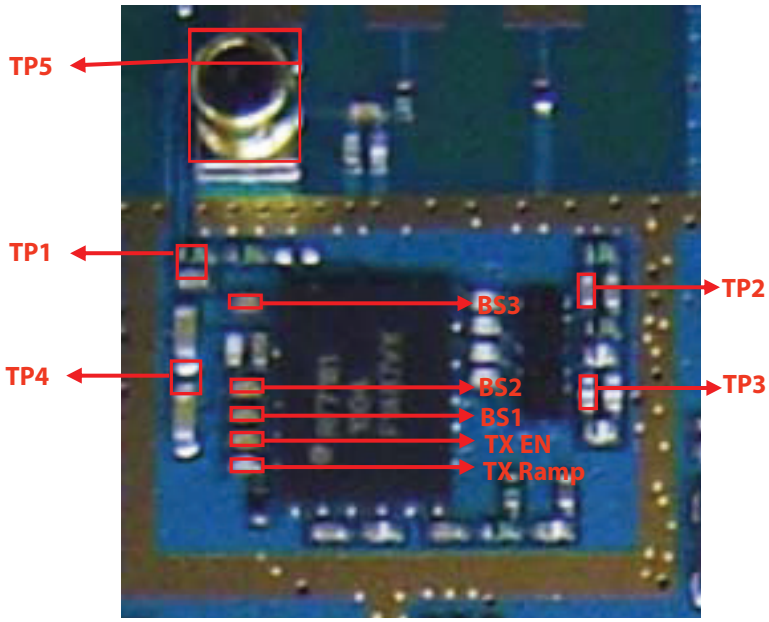
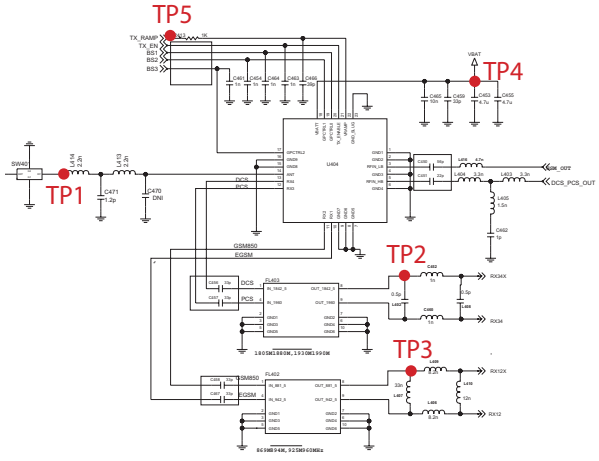


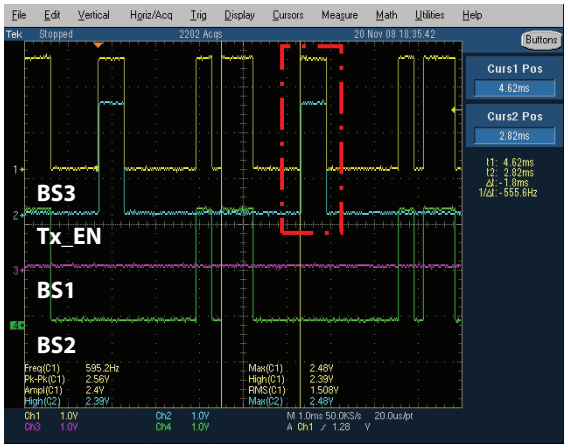
Figure 4.3.4

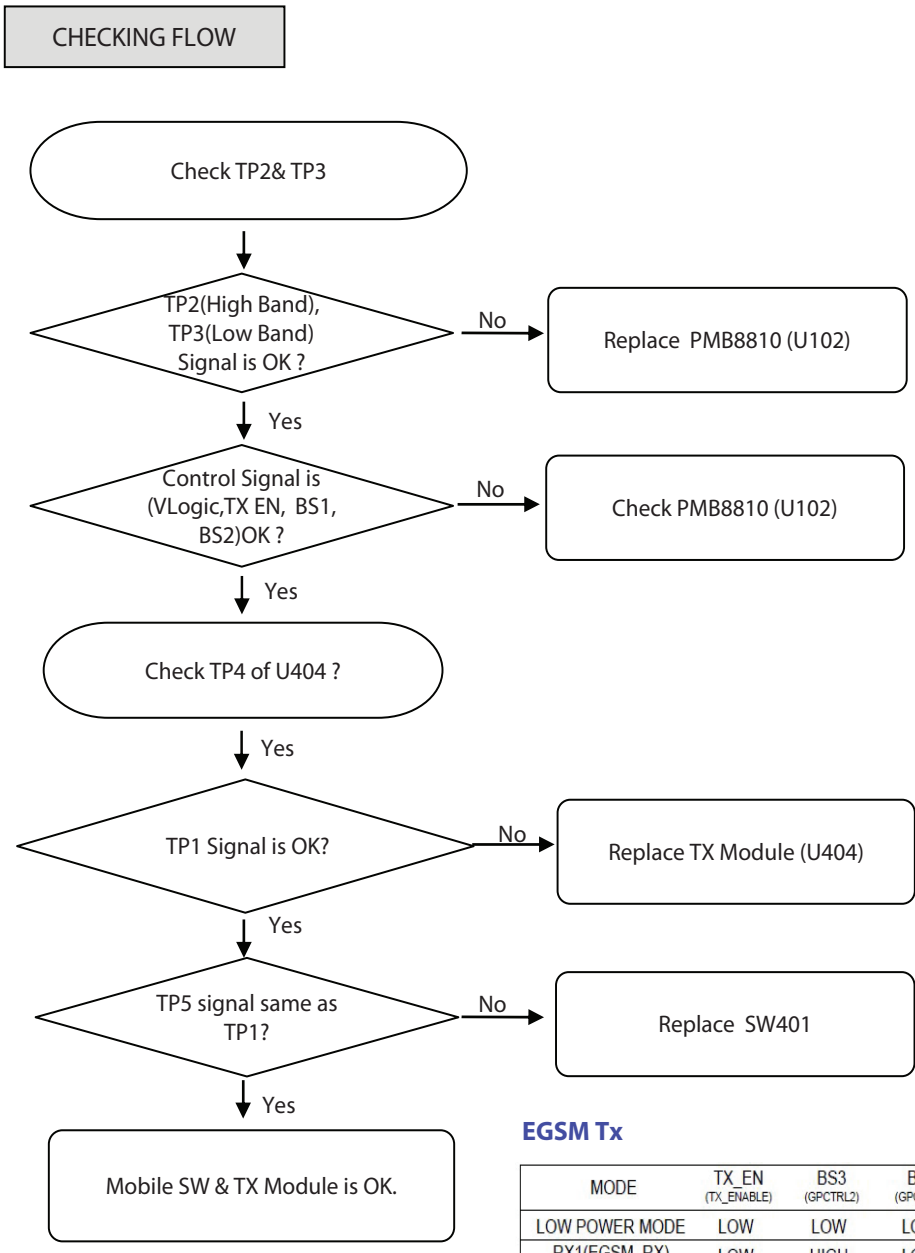
CIRCUIT



CONTROL LOGIC

EGSM Tx





EGSM Tx

MODE	TX_EN (TX_ENABLE)	BS3 (GPCTRL2)	BS2 (GPCTRL1)	BS1 (GPCTRL0)
LOW POWER MODE	LOW	LOW	LOW	LOW
RX1(EGSM_RX)	LOW	HIGH	LOW	LOW
RX2(GSM850_RX)	LOW	LOW	HIGH	LOW
RX3(PCS_RX)	LOW	LOW	HIGH	HIGH
RX4(DCS_RX)	LOW	LOW	LOW	HIGH
GSM850/900_TX	HIGH	LOW	HIGH	LOW
DCS/PCS_TX	HIGH	LOW	HIGH	HIGH

4.4 Power On Trouble

TEST POINT

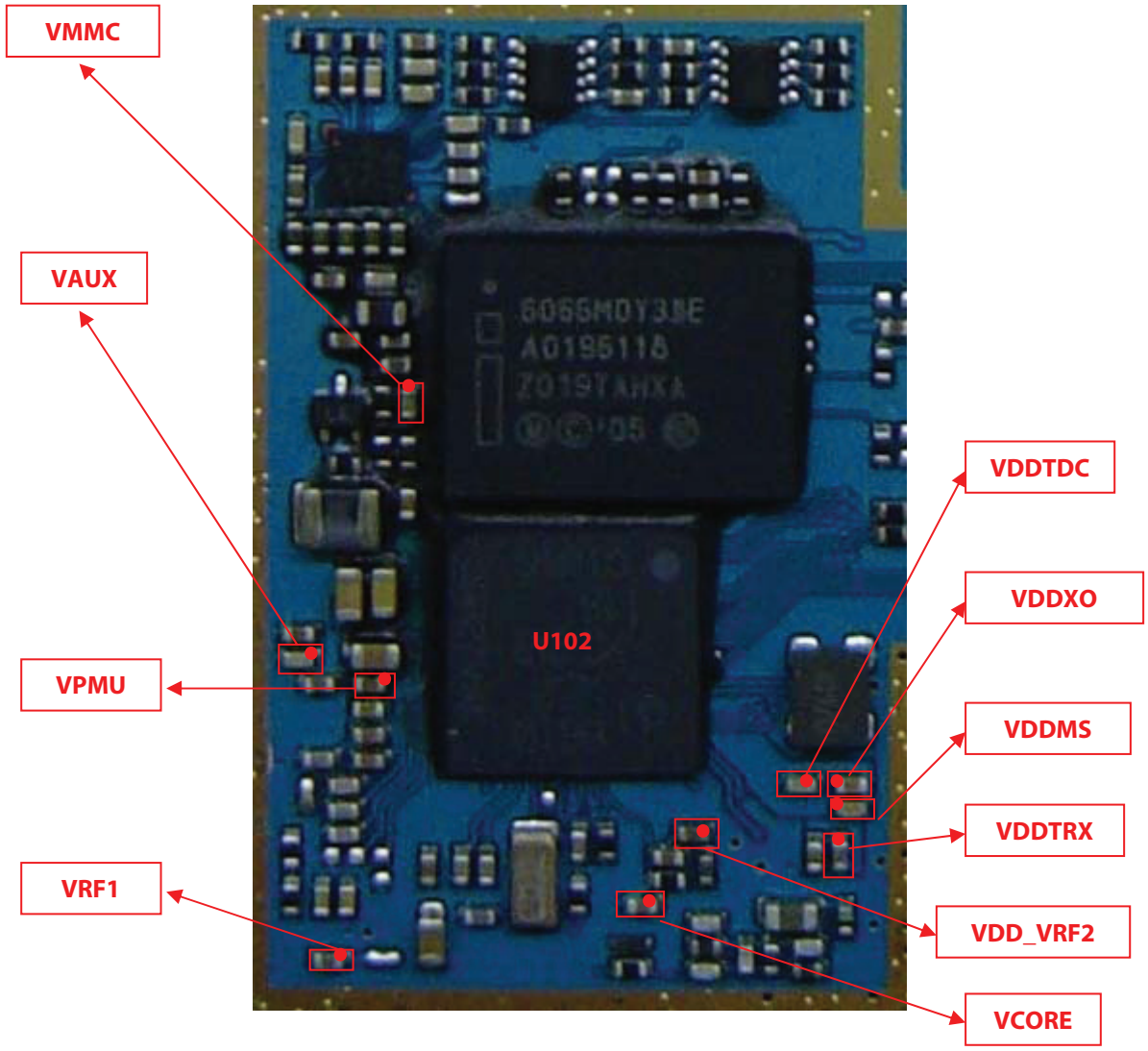


Figure 4.1

CIRCUIT

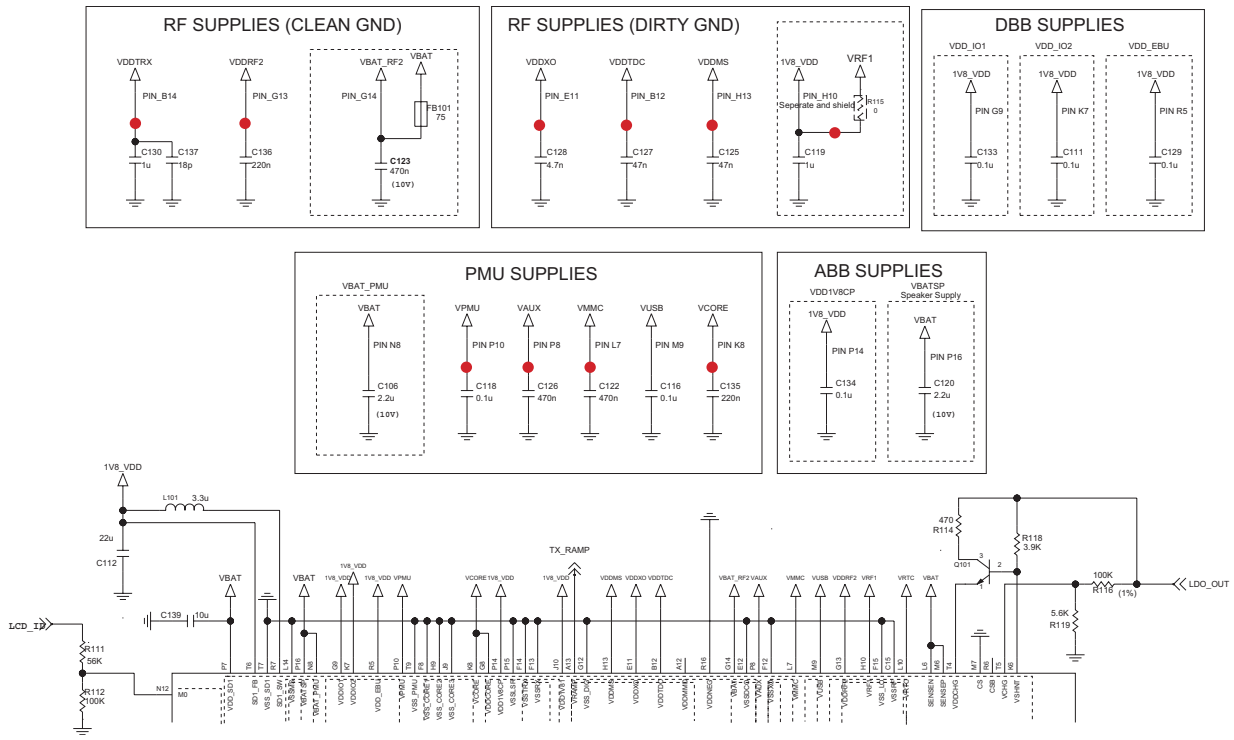
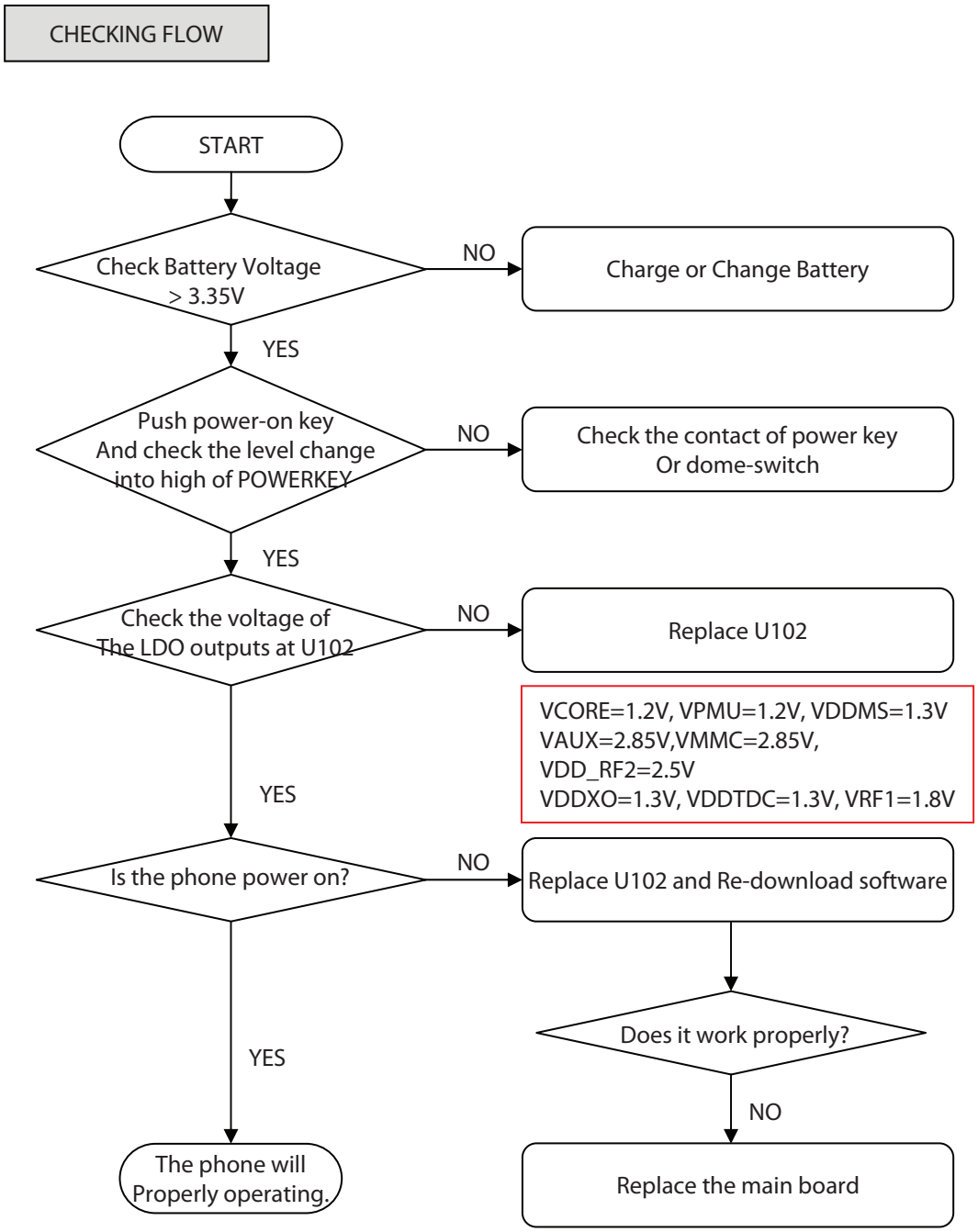


Figure 4.2 Power block of LG-T310i



4.5 Charging Trouble

TEST POINT

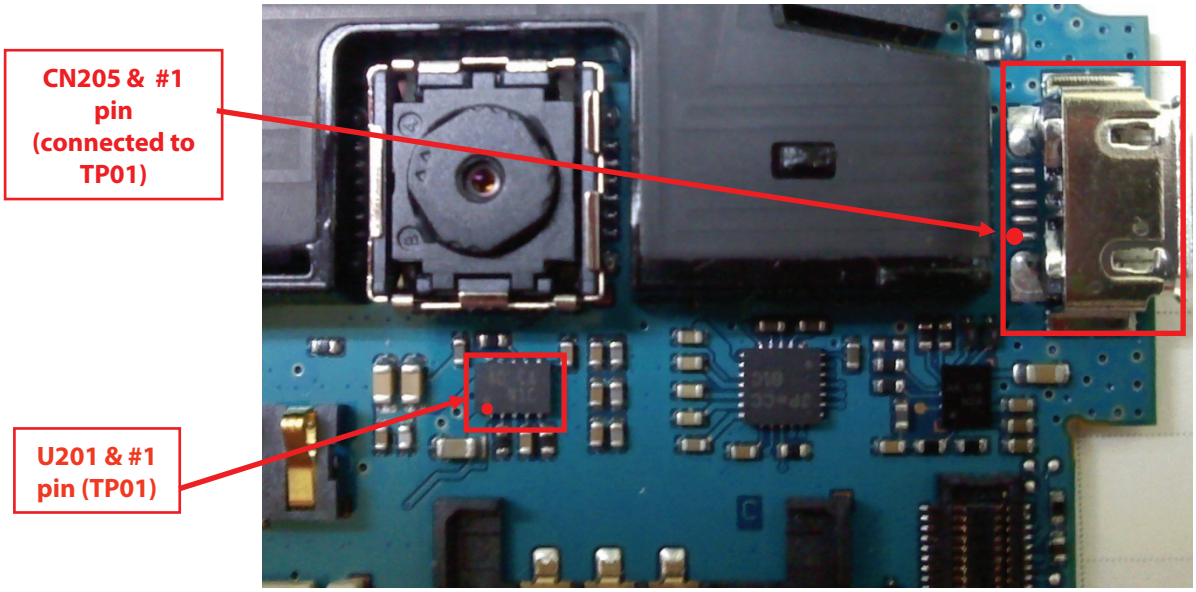
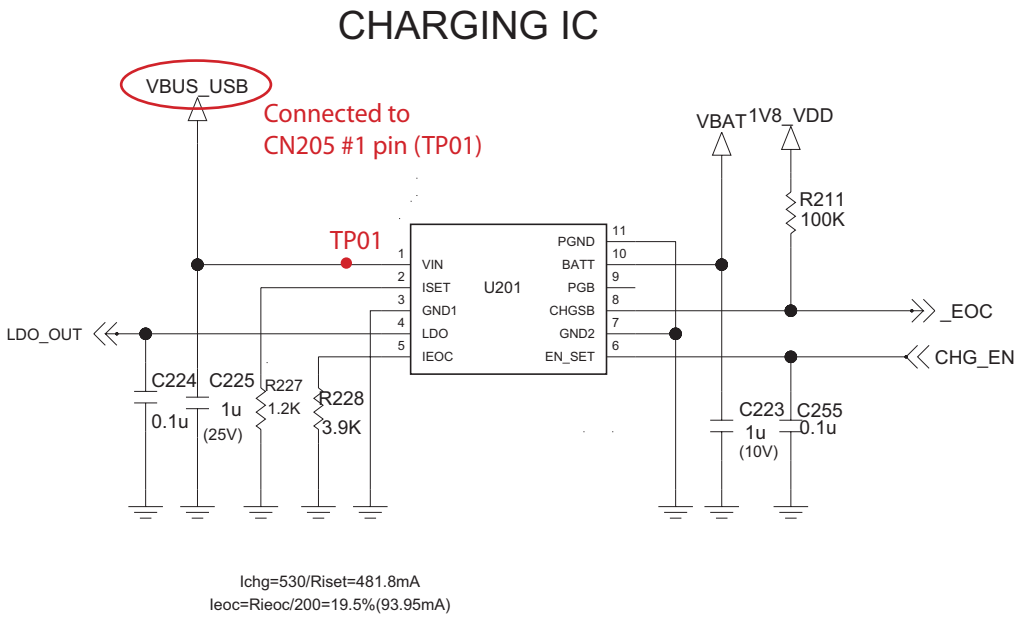
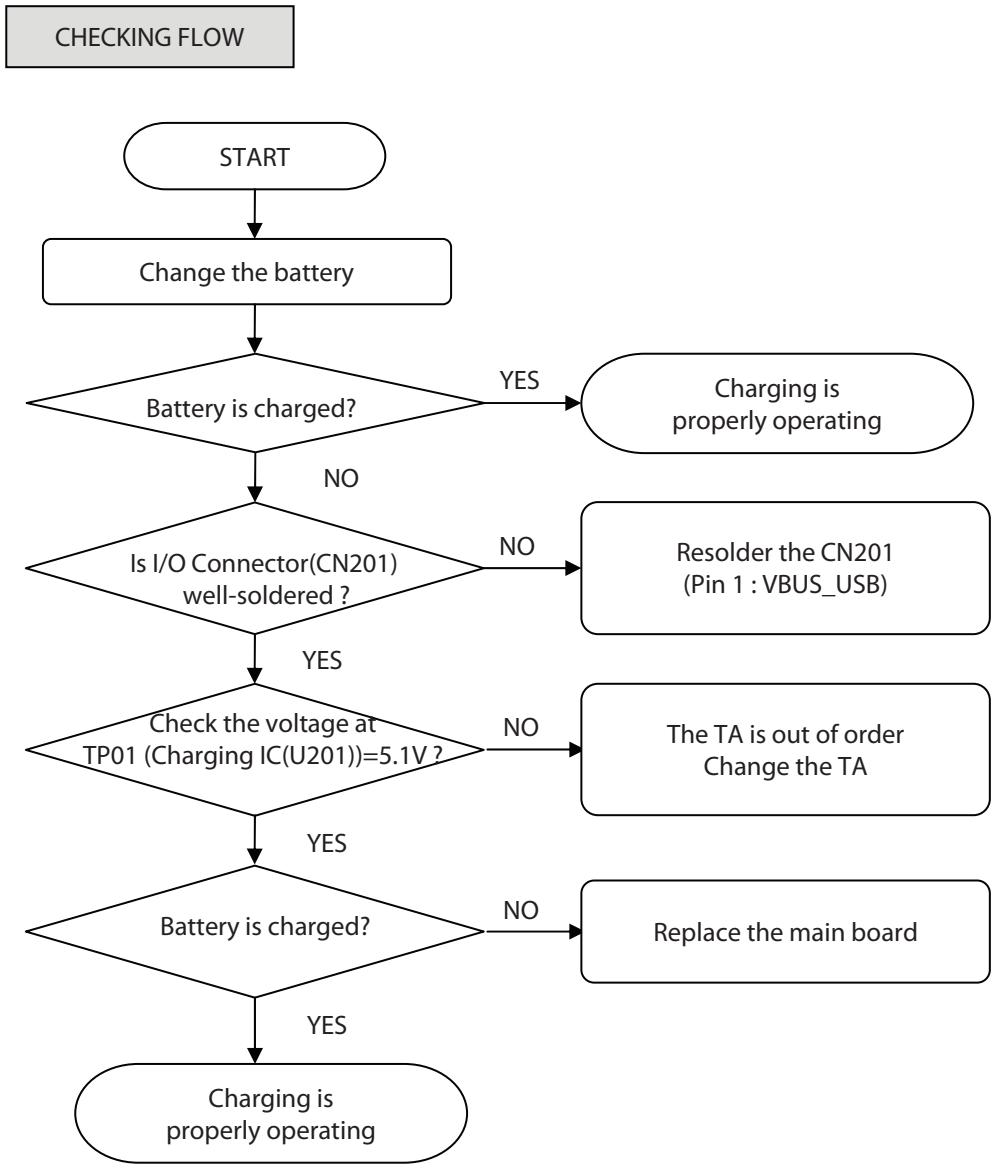


Figure 4.5

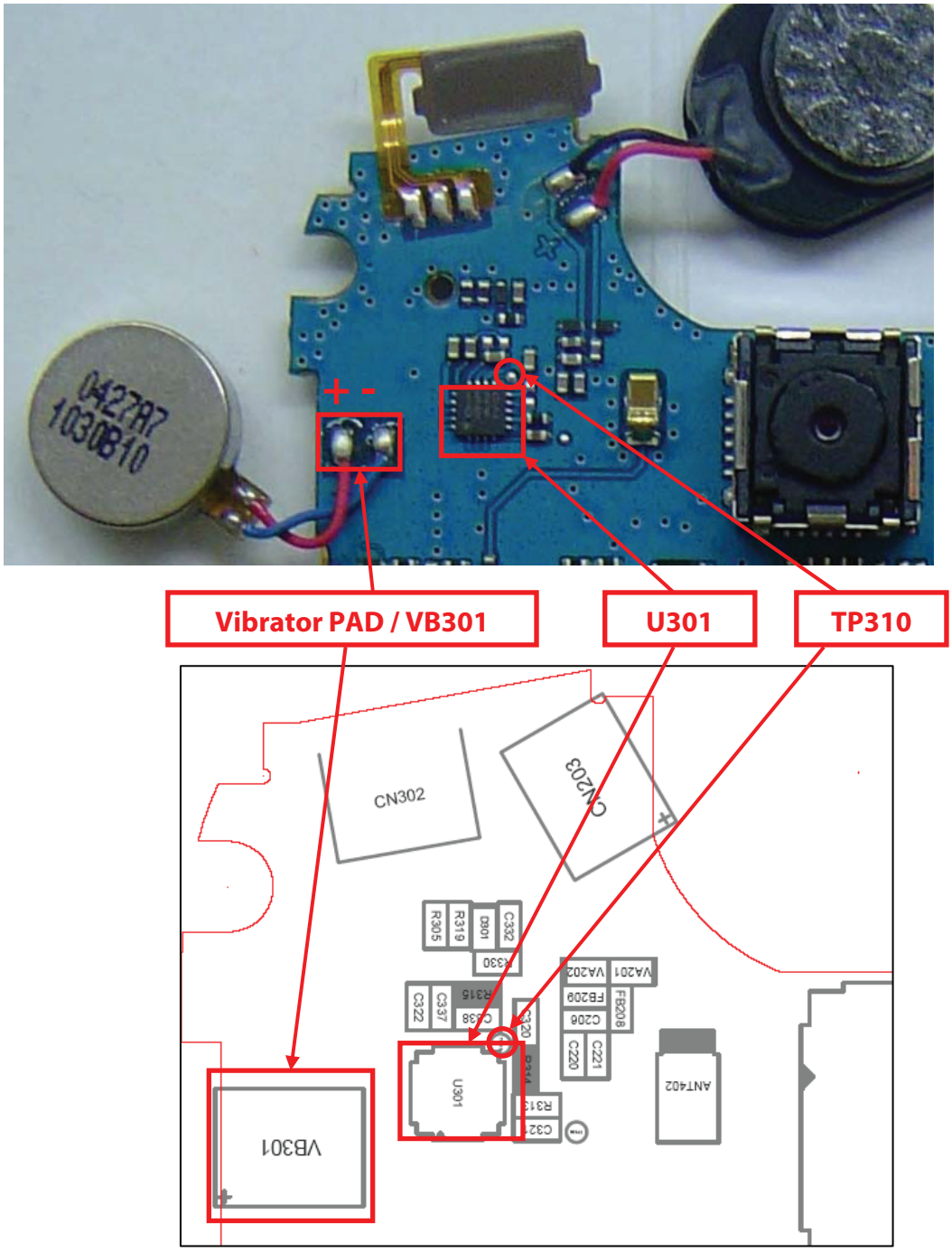
CIRCUIT



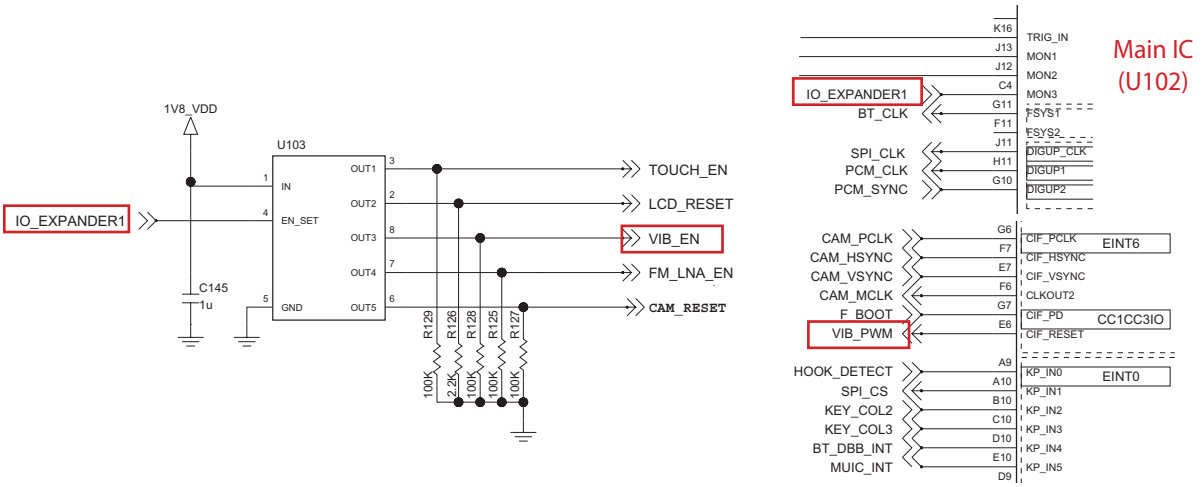


4.6 Vibrator Trouble

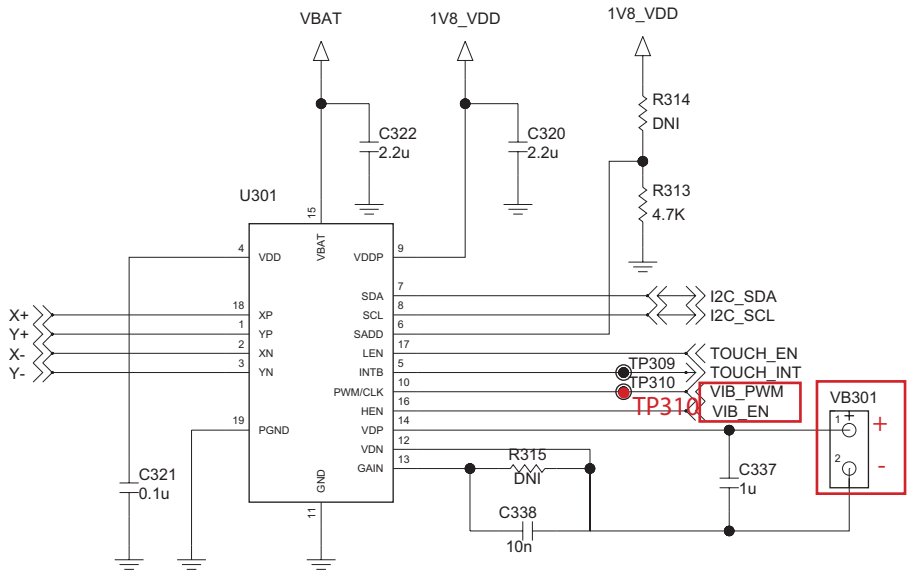
TEST POINT



CIRCUIT

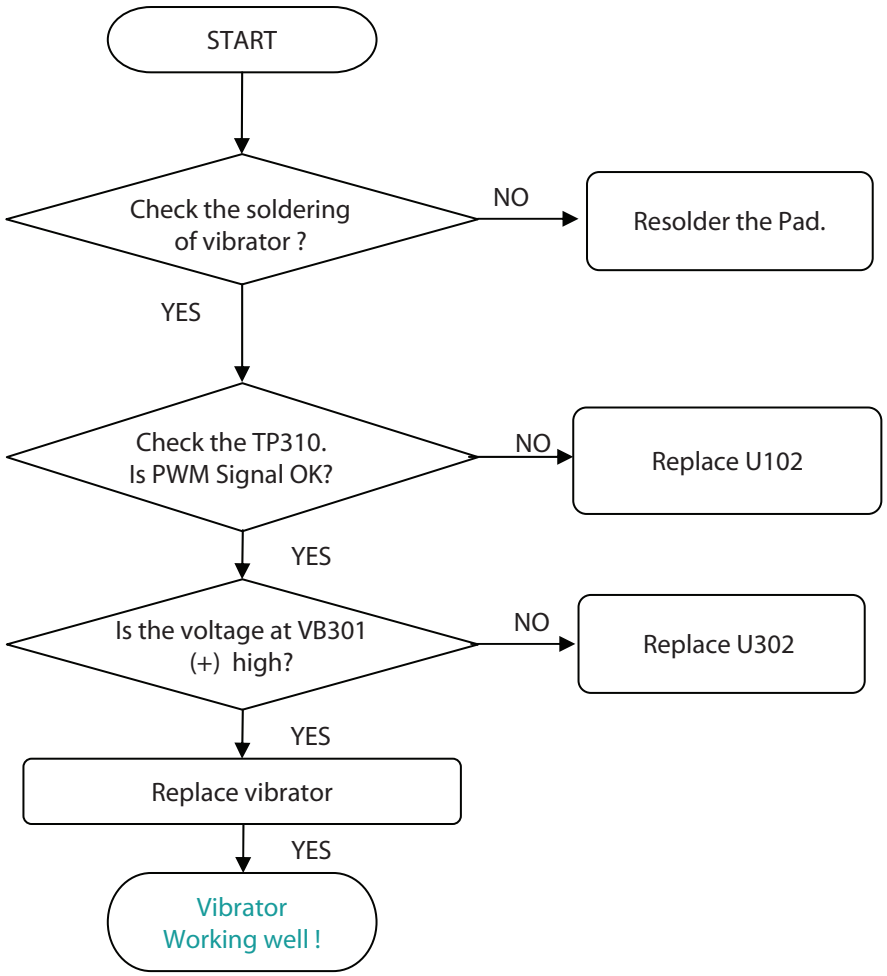


Touch & Haptic Driver Ckts



CHECKING FLOW

SETTING : Enter the engineering mode, and set vibrator on at vibration of BB test menu



4.7 LCD Trouble

TEST POINT

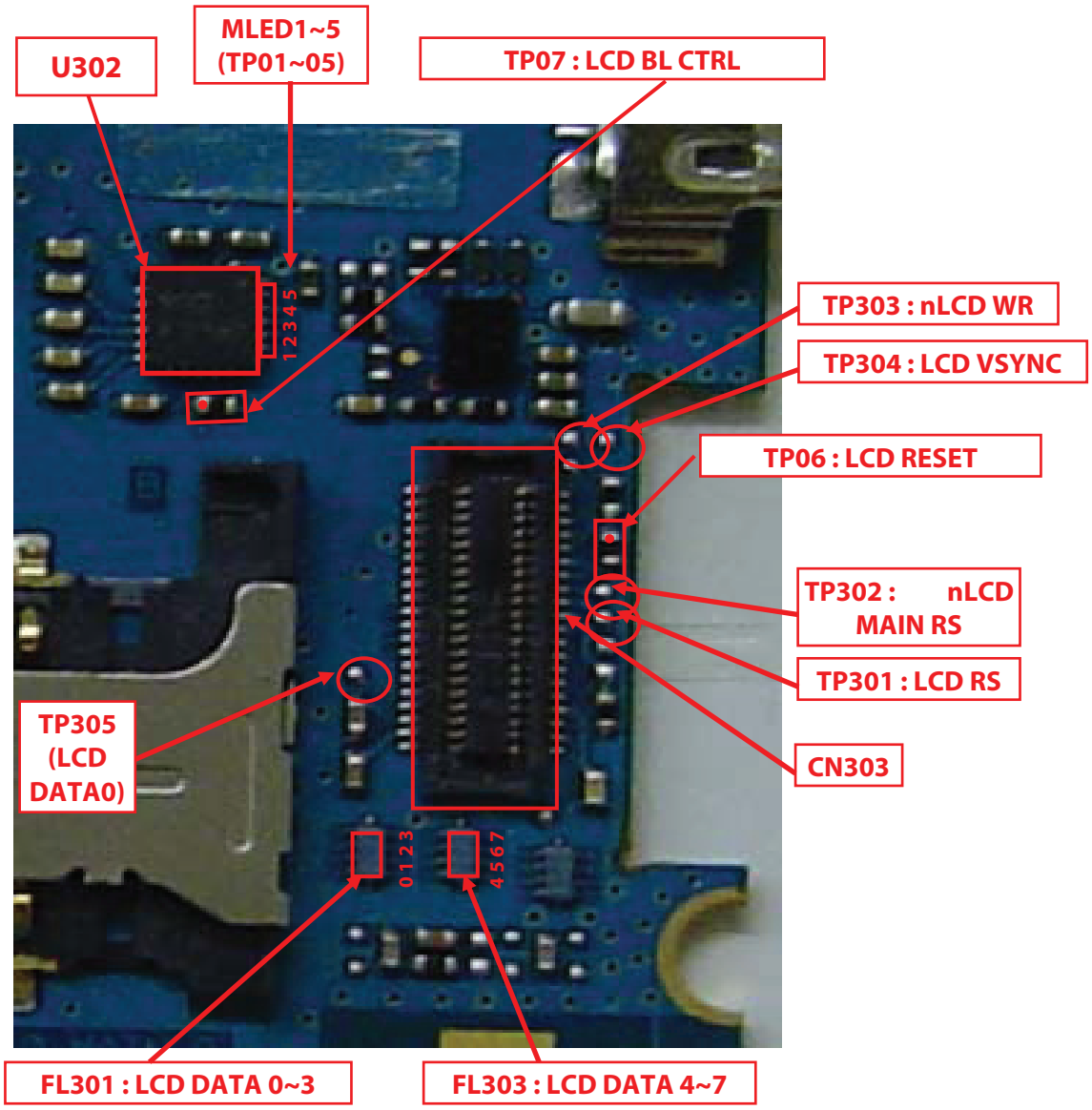
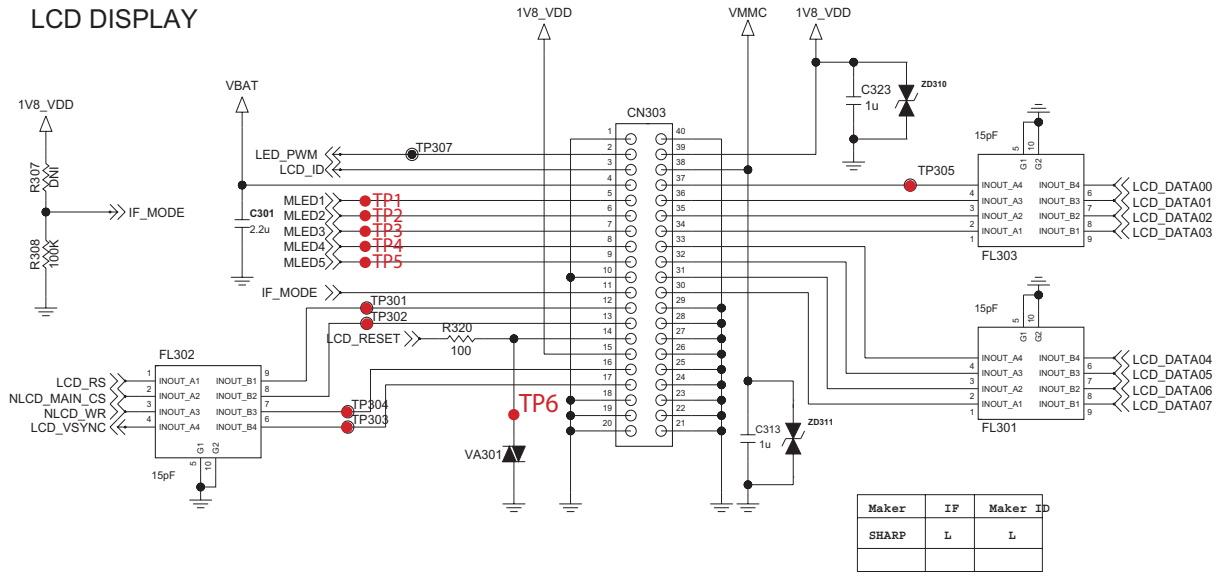
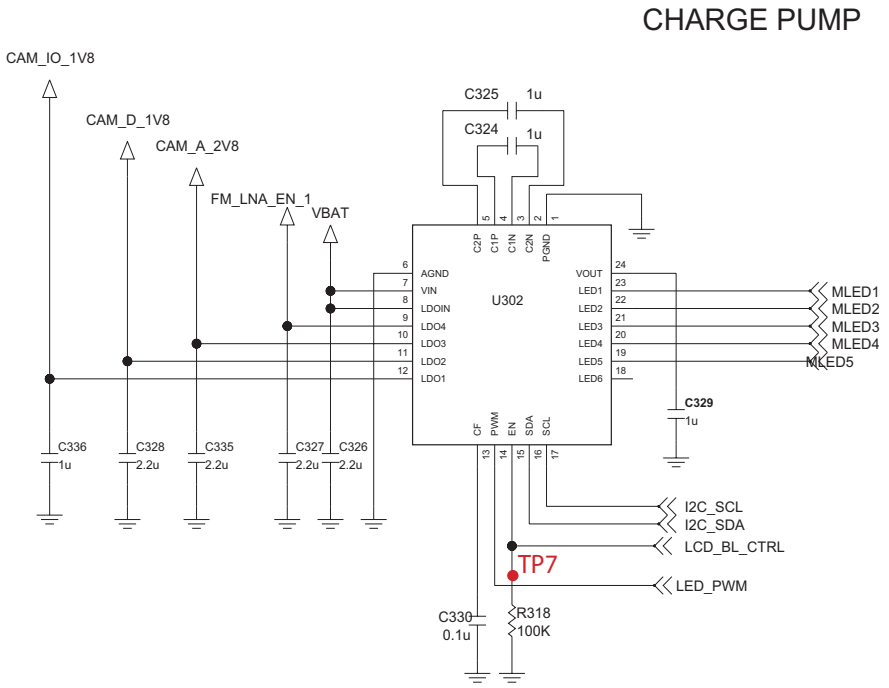


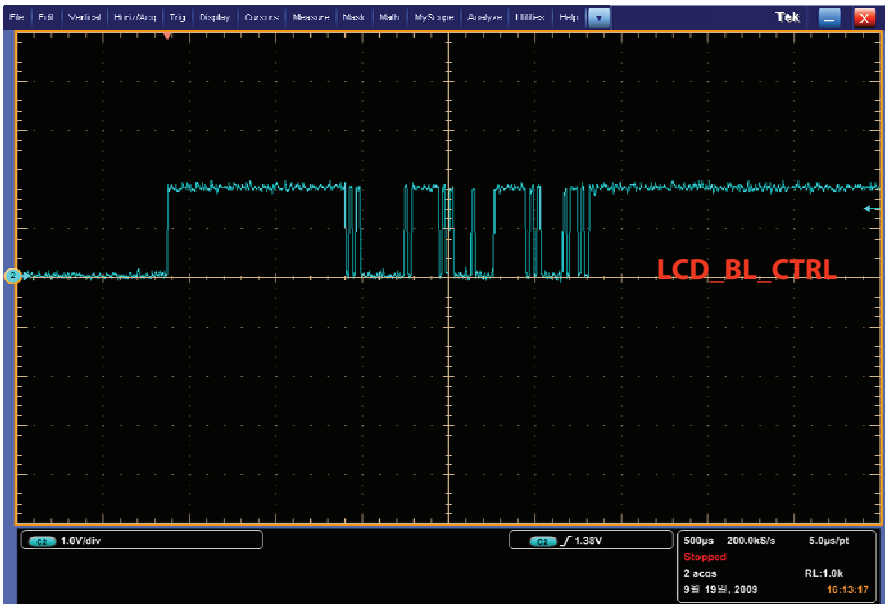
Figure 4.7

CIRCUIT

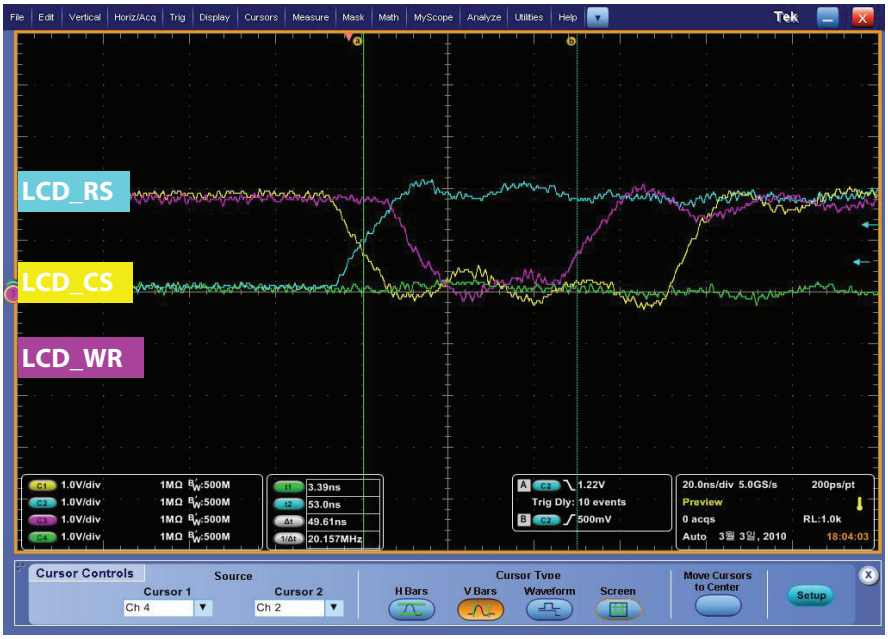




Waveform

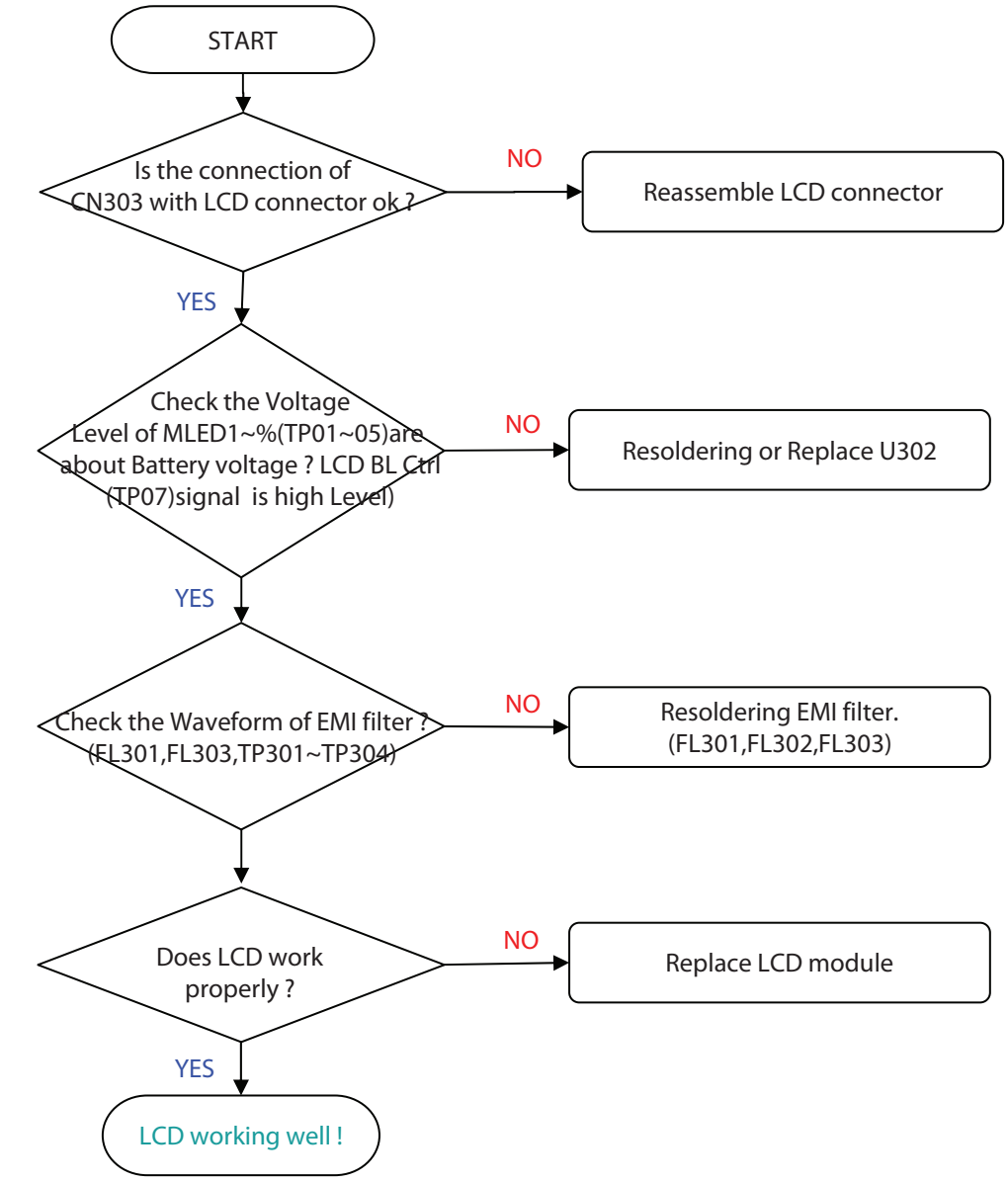


Graph 4.7.1. LCD Backlight Control Signal Waveform



Graph 4.7.2. LCD Data Waveform

CHECKING FLOW



4.8 Camera Trouble

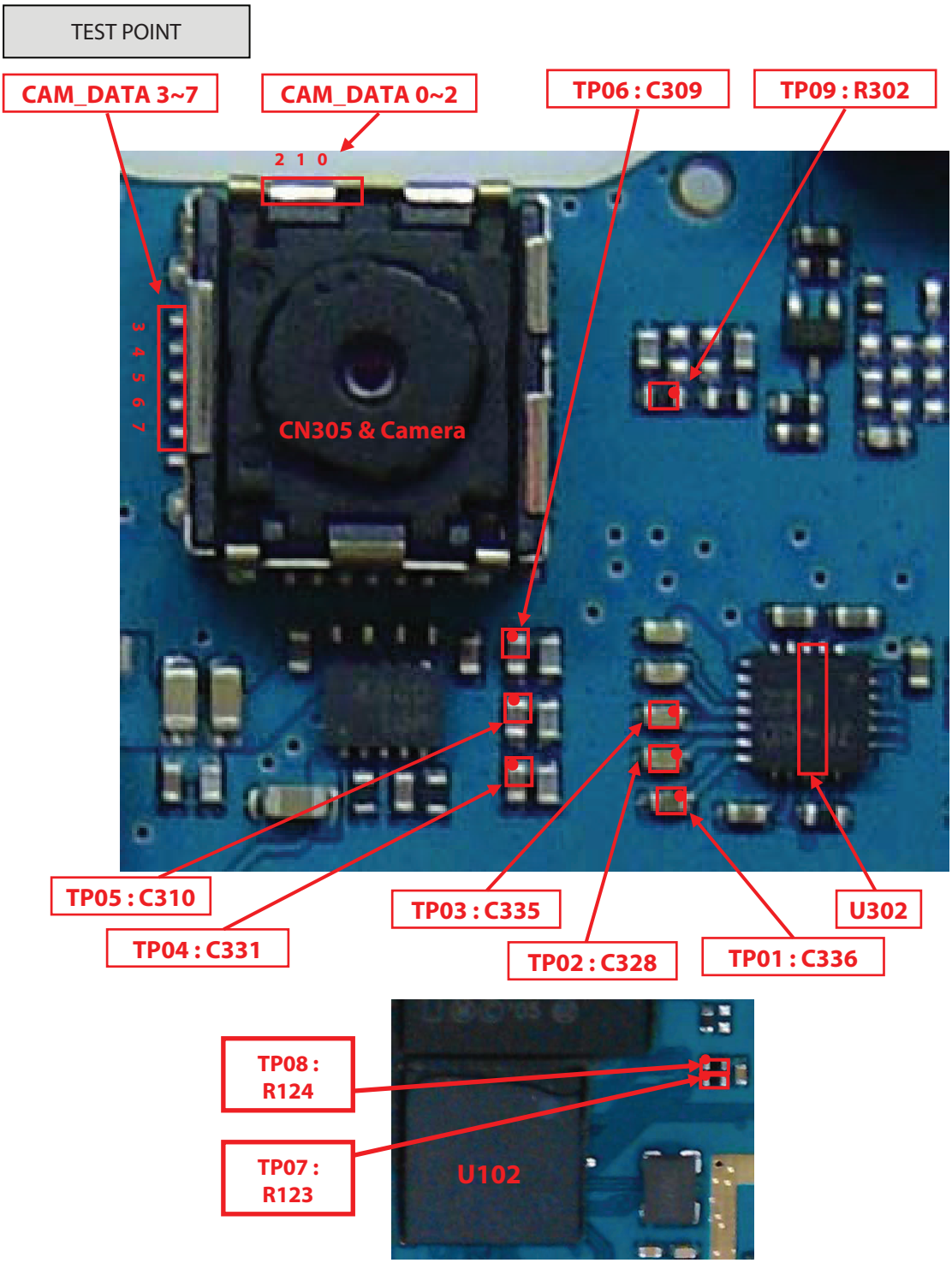
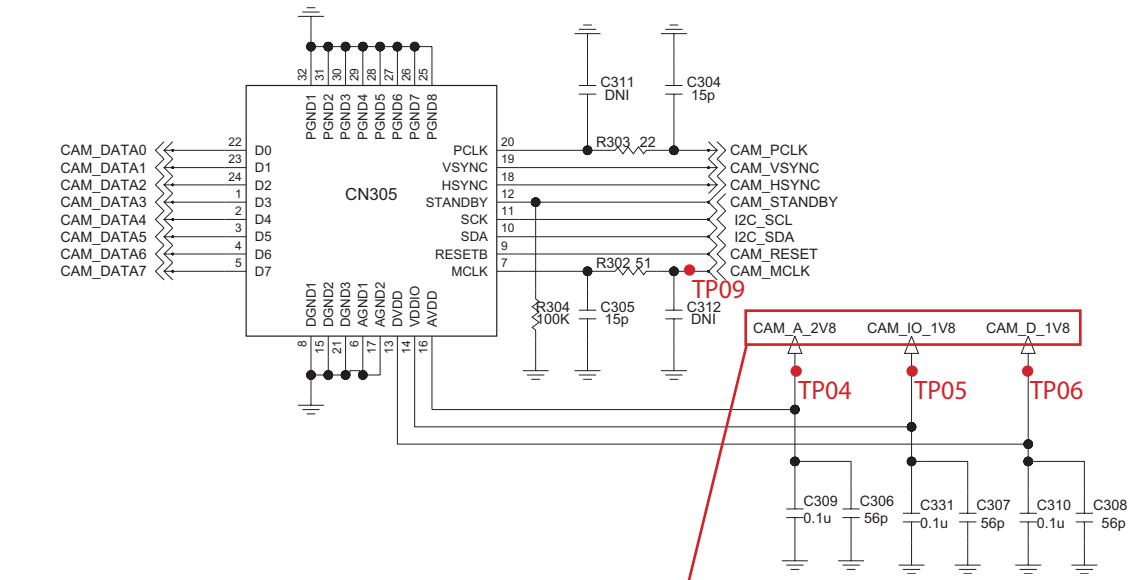


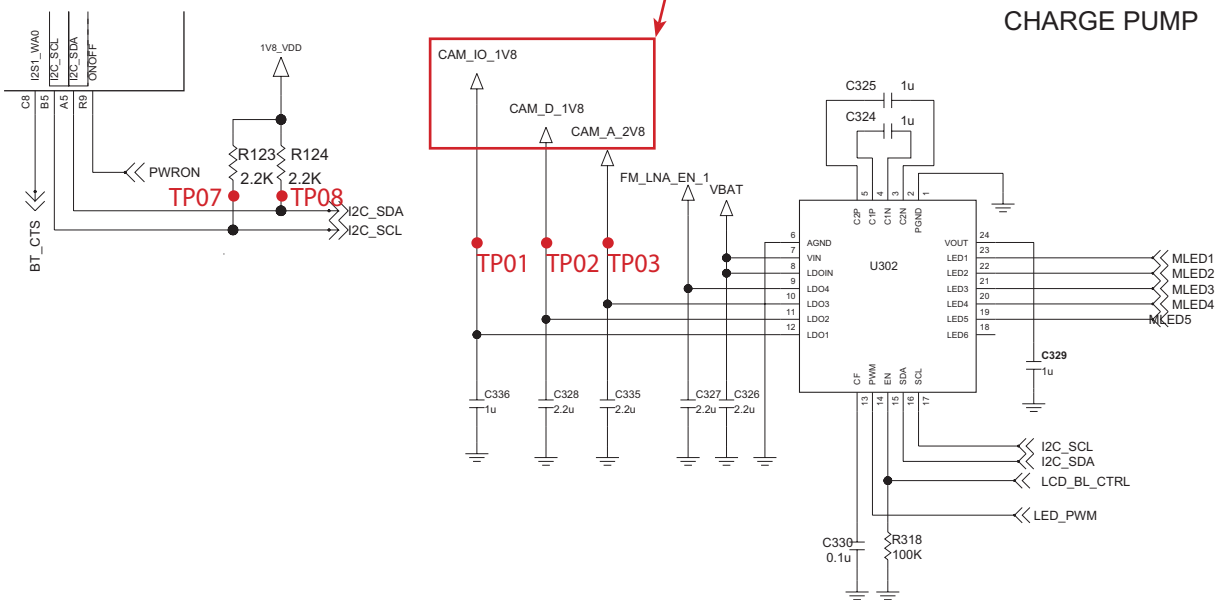
Figure 4.8

CIRCUIT

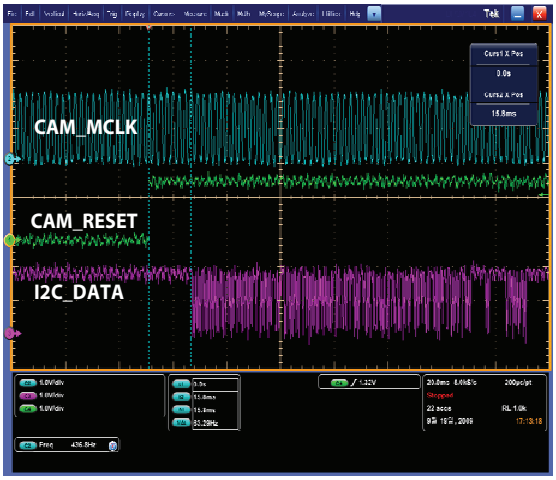
CAMERA INTERFACE



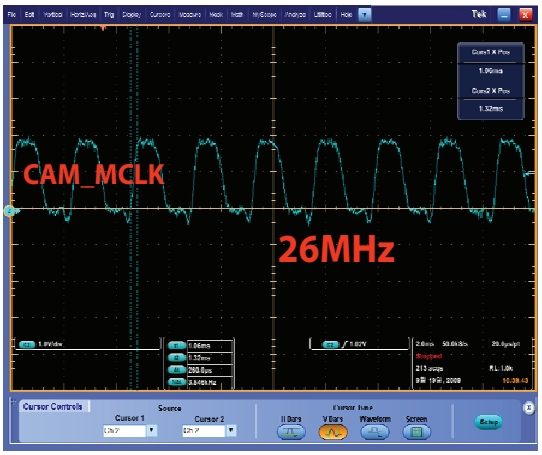
CHARGE PUMP



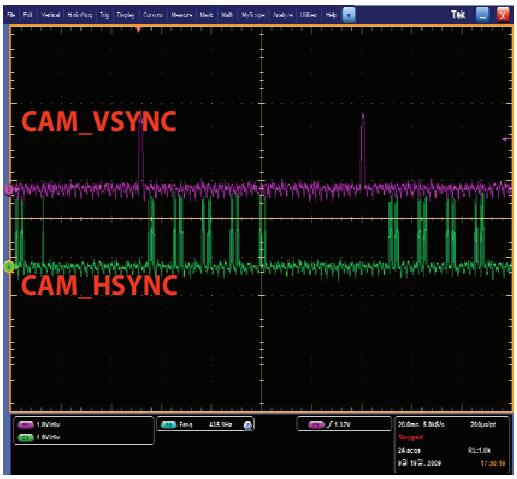
Waveform



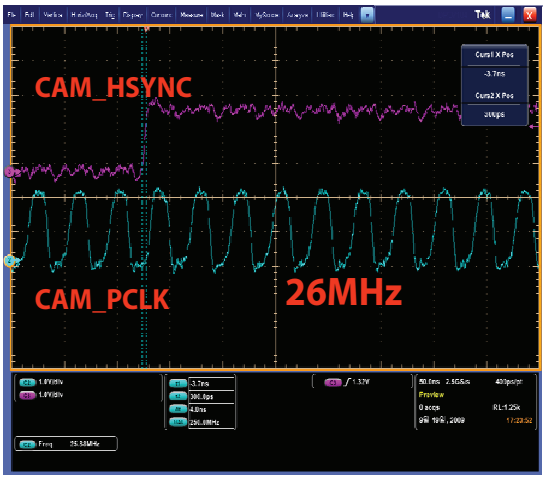
Graph 4.8.1. I2C Data Waveform



Graph 4.8.2. MCLK Waveform

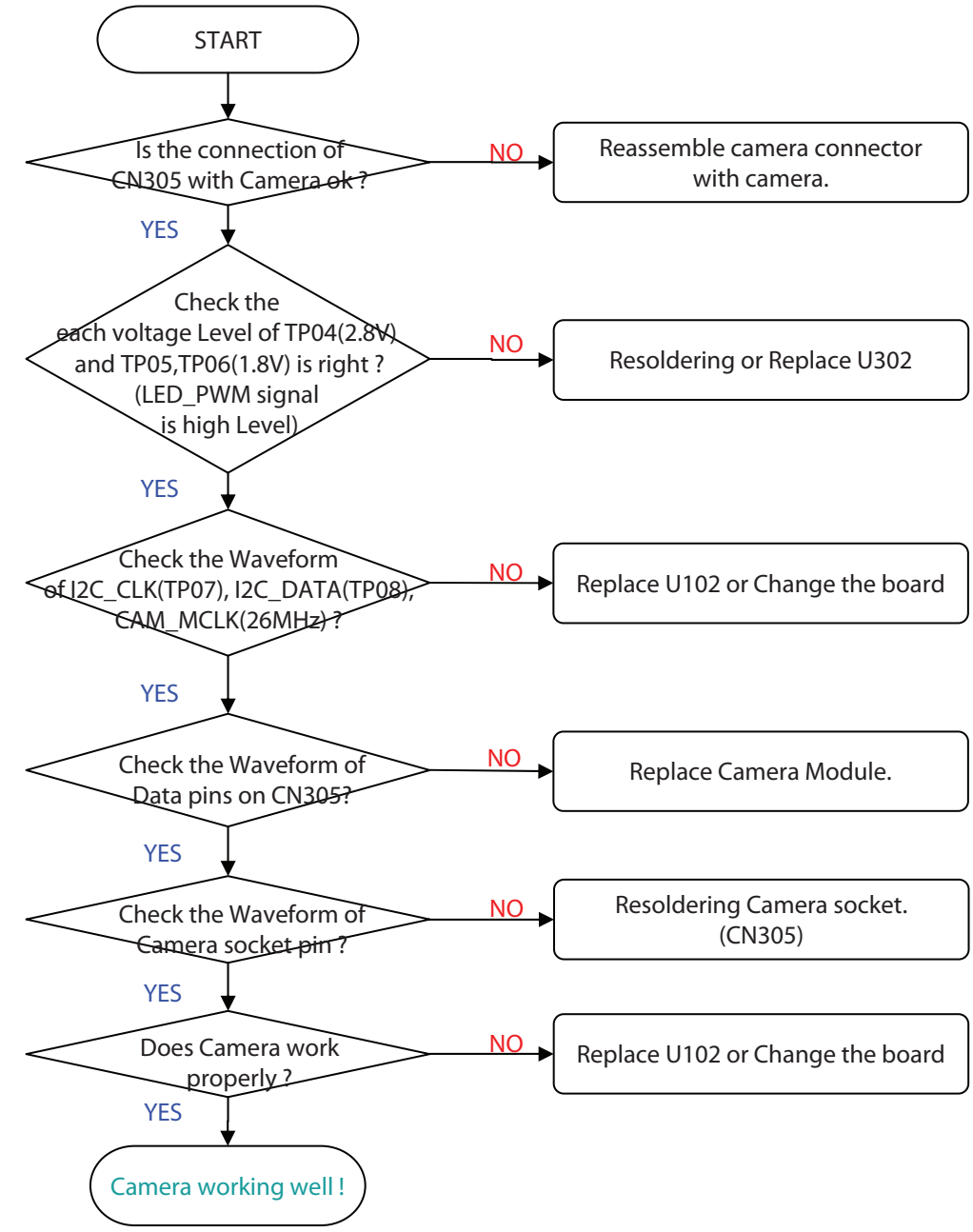


Graph 4.8.3.CAM_VSYNC vs. CAM_HSYNC Waveform



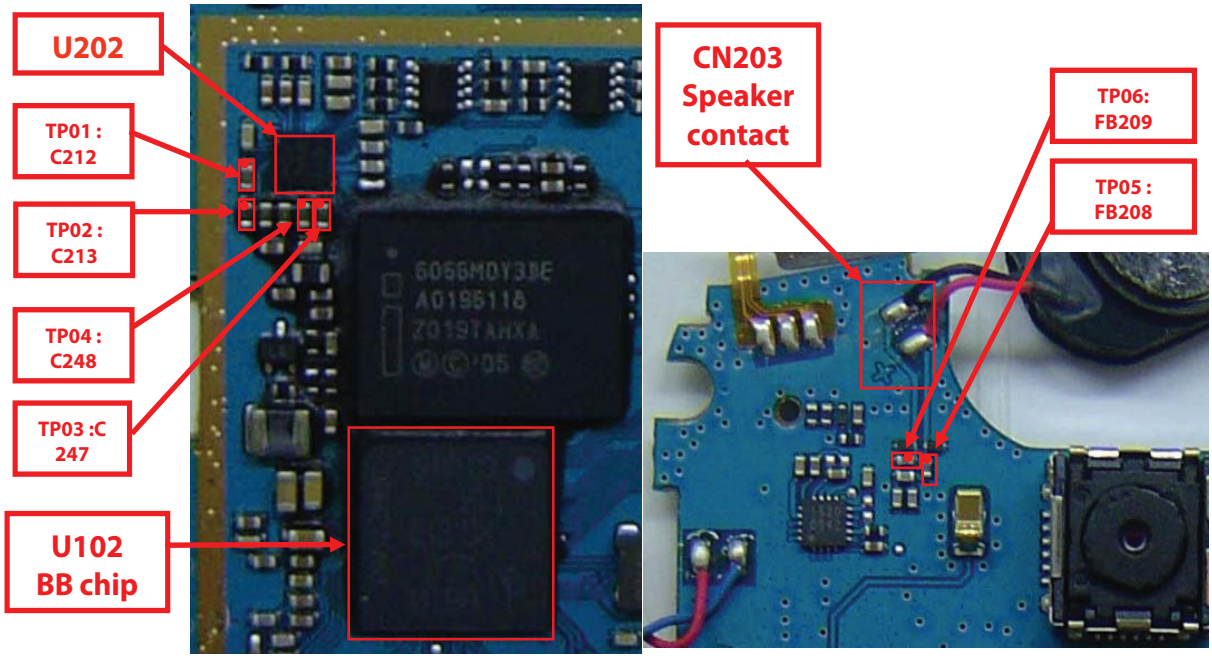
Graph 4.8.4.CAM_HSYNC vs. CAM_PCLK Waveform

CHECKING FLOW

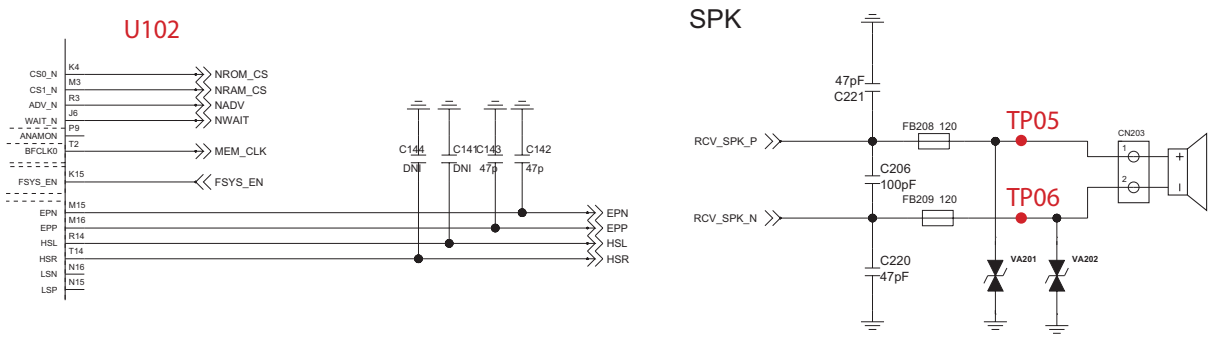


4.9 Speaker / Receiver Trouble

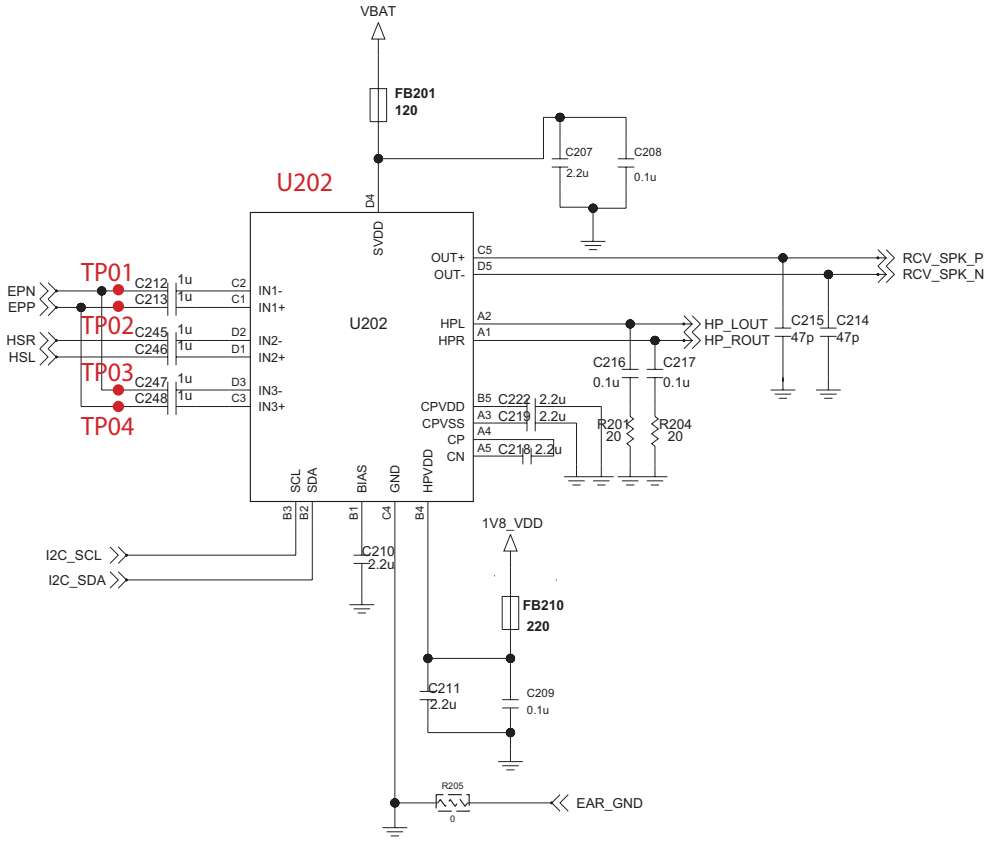
TEST POINT



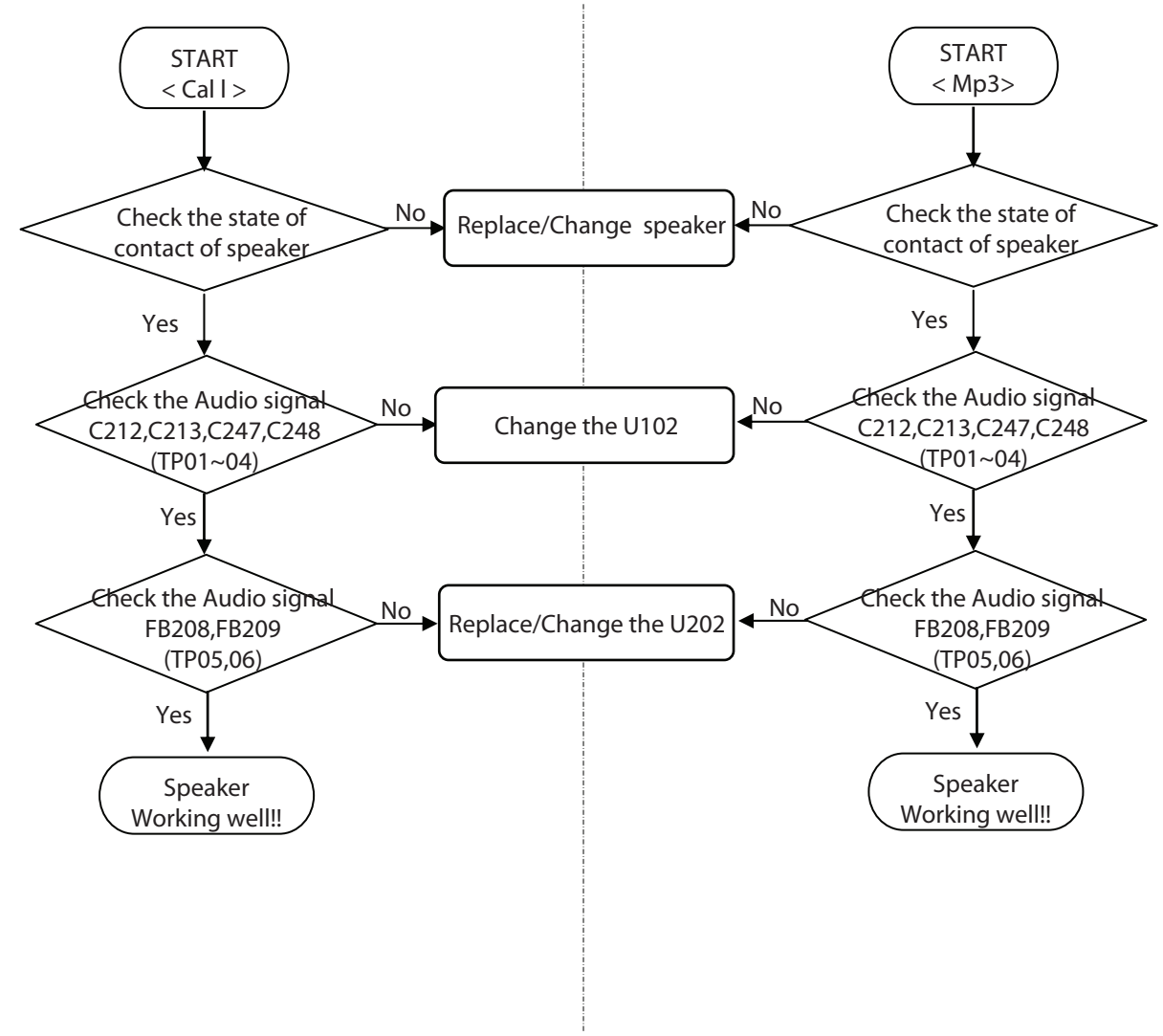
CIRCUIT



AUDIO AMP SUB SYSTEM & SIGNAL DISTRIBUTOR

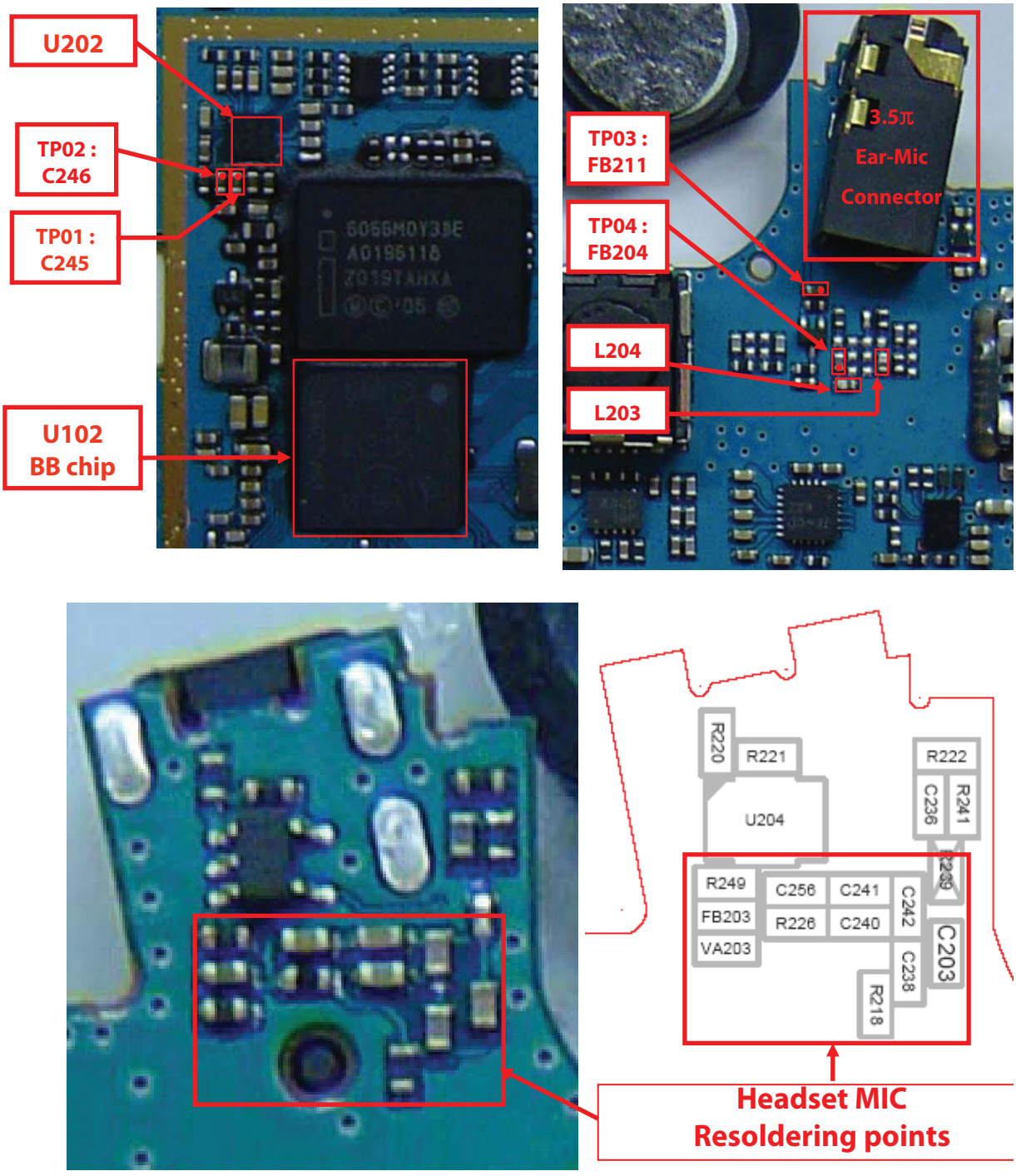


CHECKING FLOW

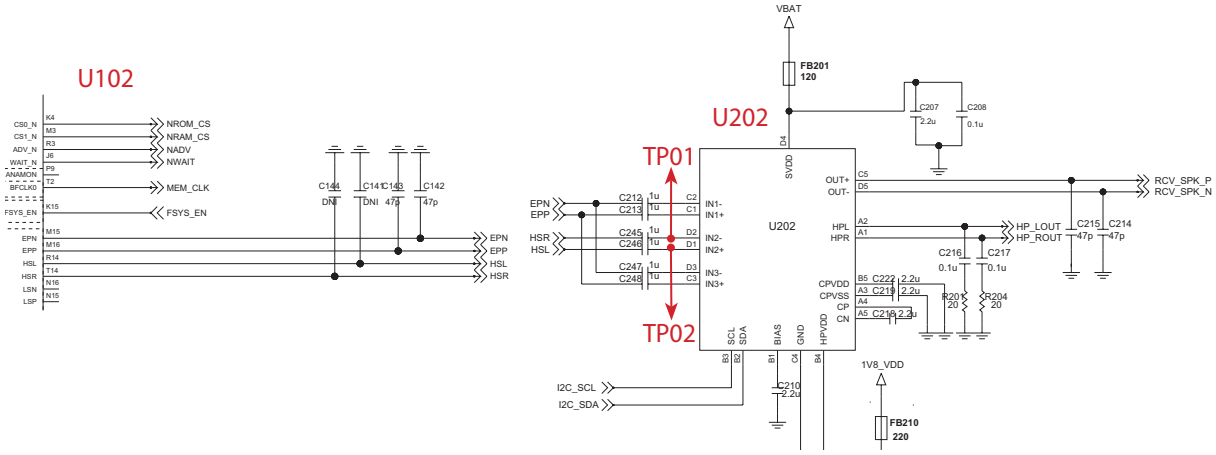


4.10 Earphone Trouble

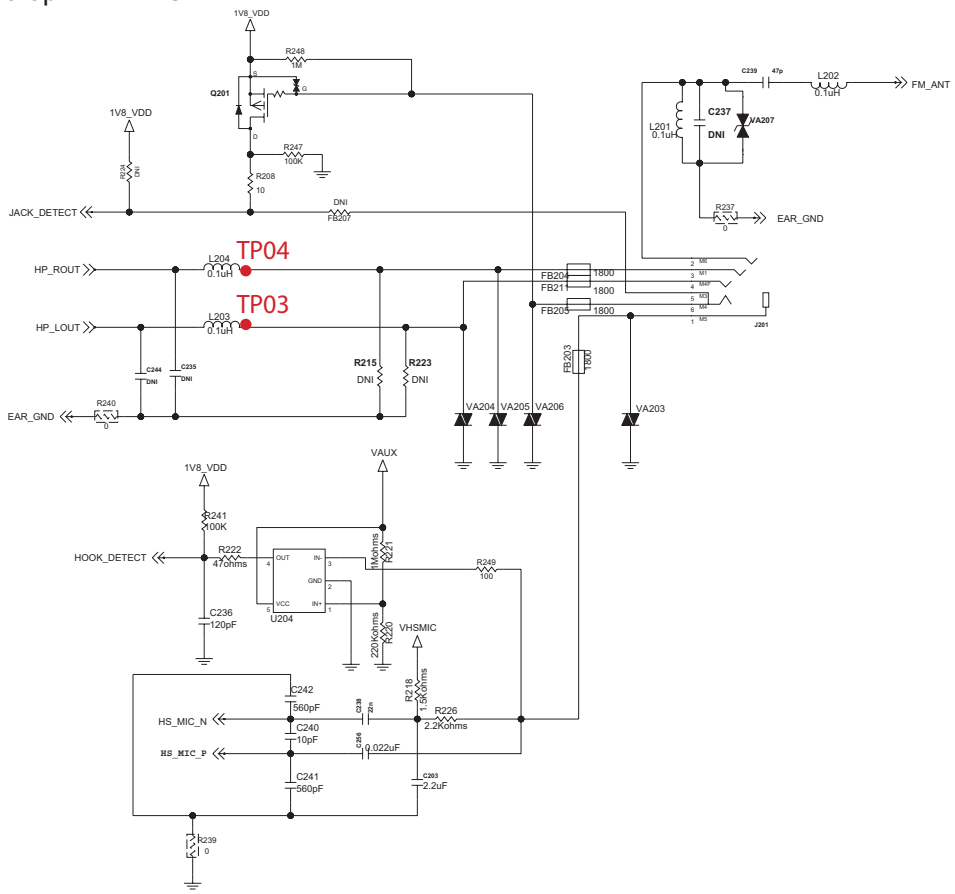
TEST POINT

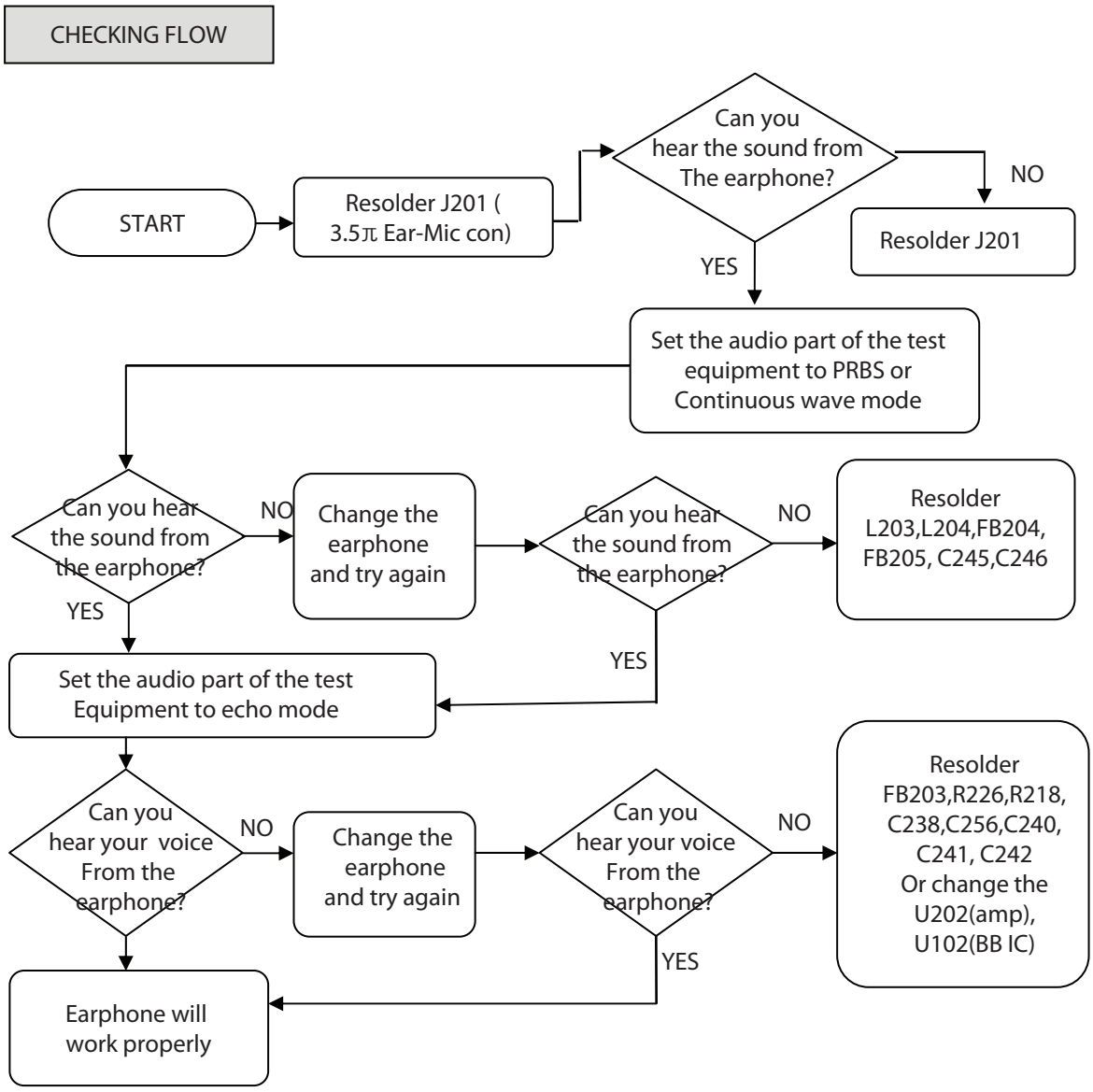


CIRCUIT



3.5phi HEADSET





4.11 Microphone Trouble

TEST POINT

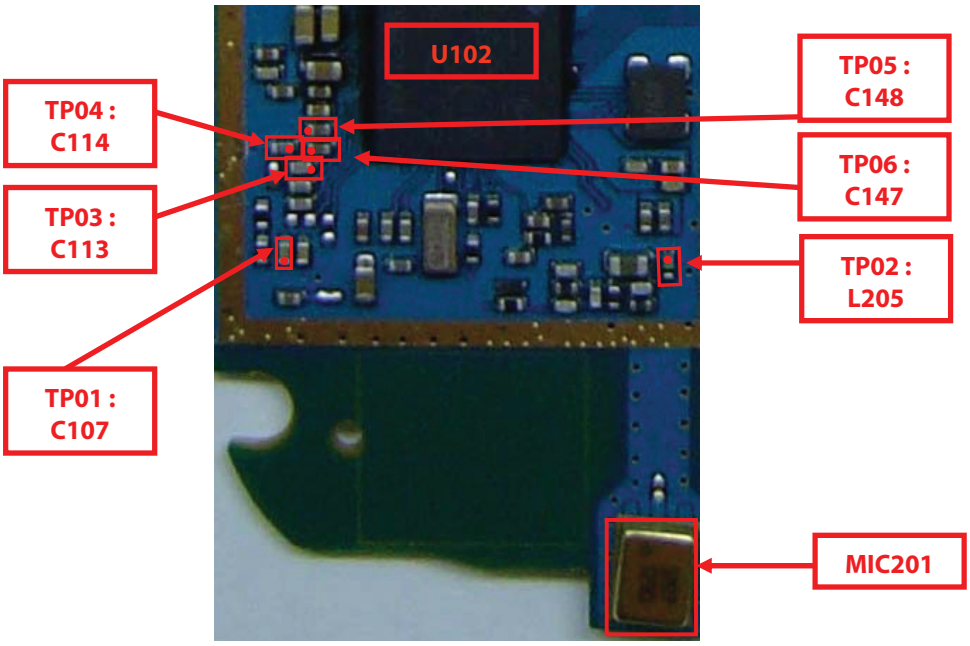
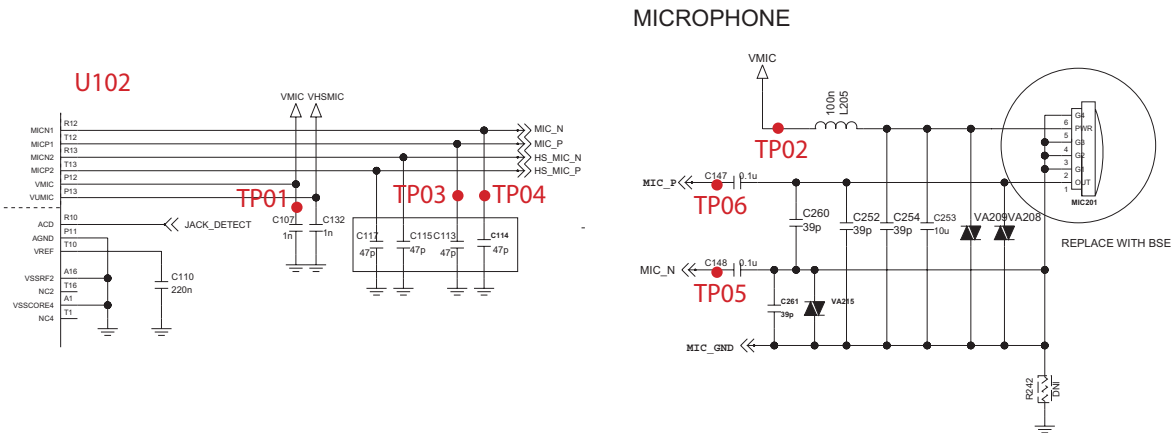


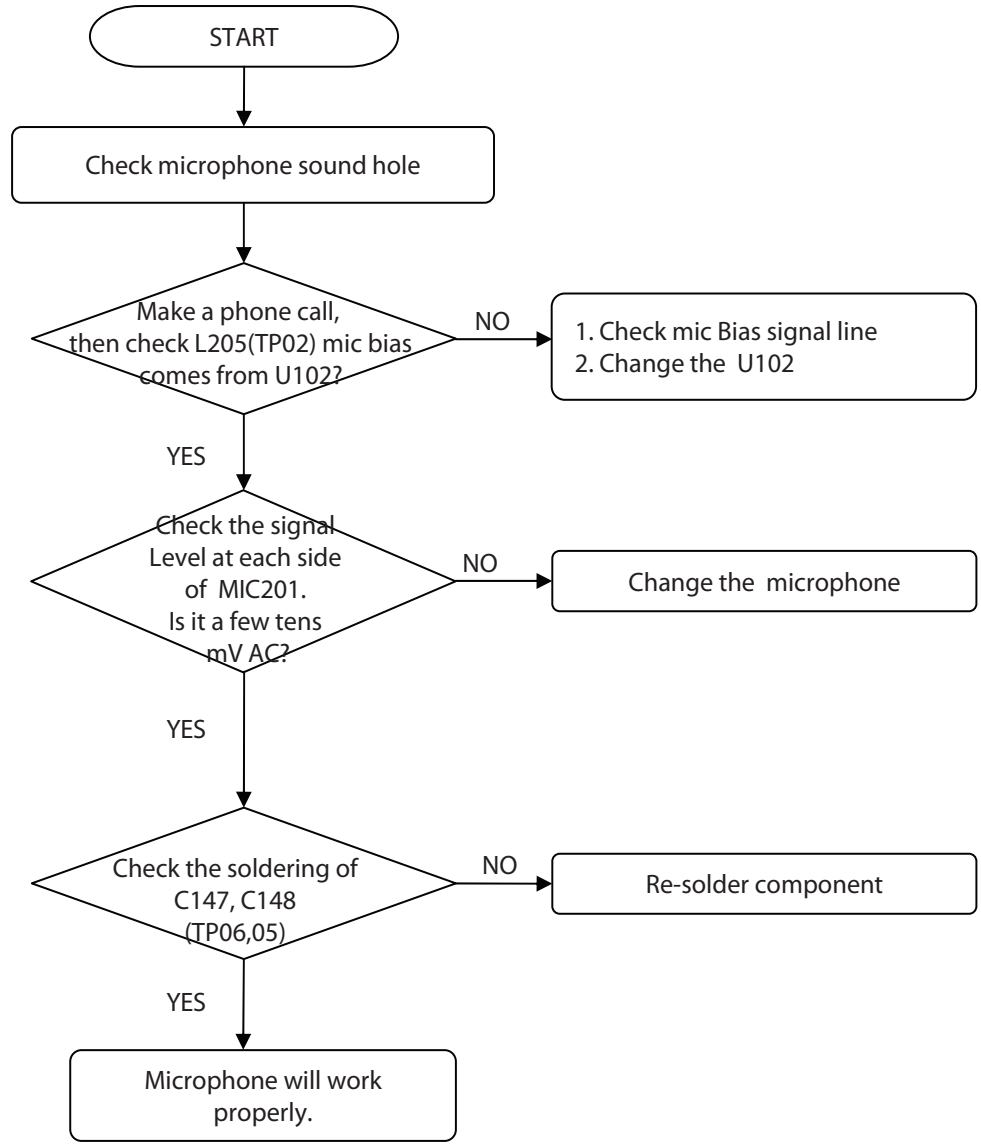
Figure 4.12

CIRCUIT



CHECKING FLOW

SETTING : After initialize Agilent 8960, Test EGSM900, DCS mode (or GSM850, PCS mode)



4.12 SIM Card Interface Trouble

TEST POINT

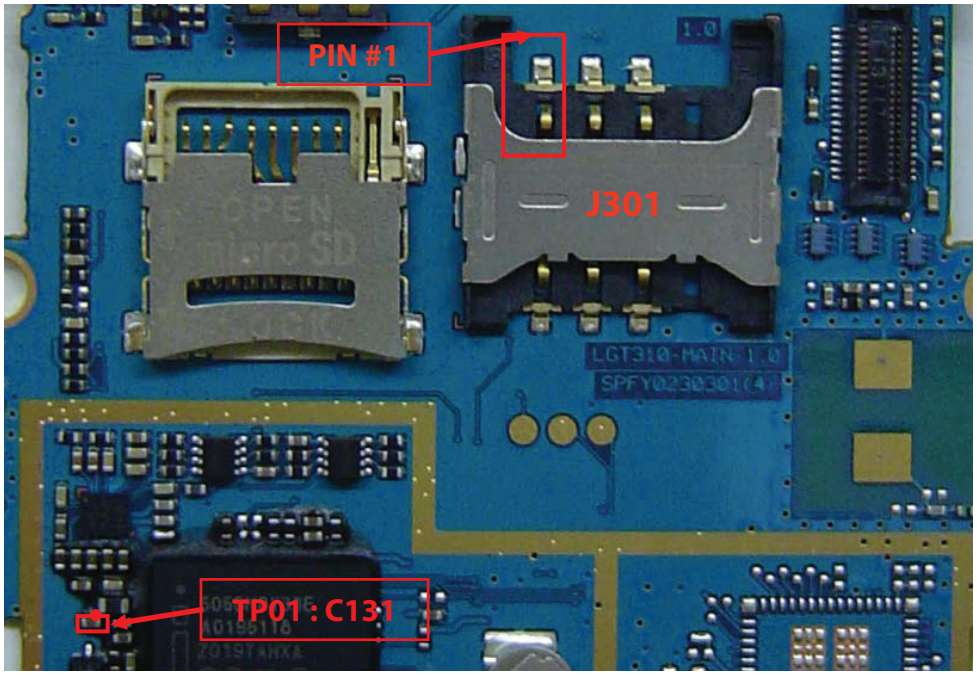
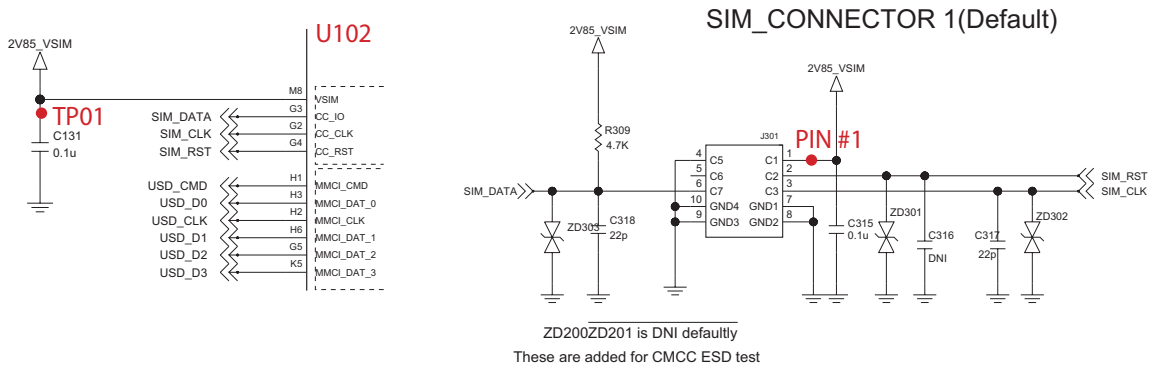
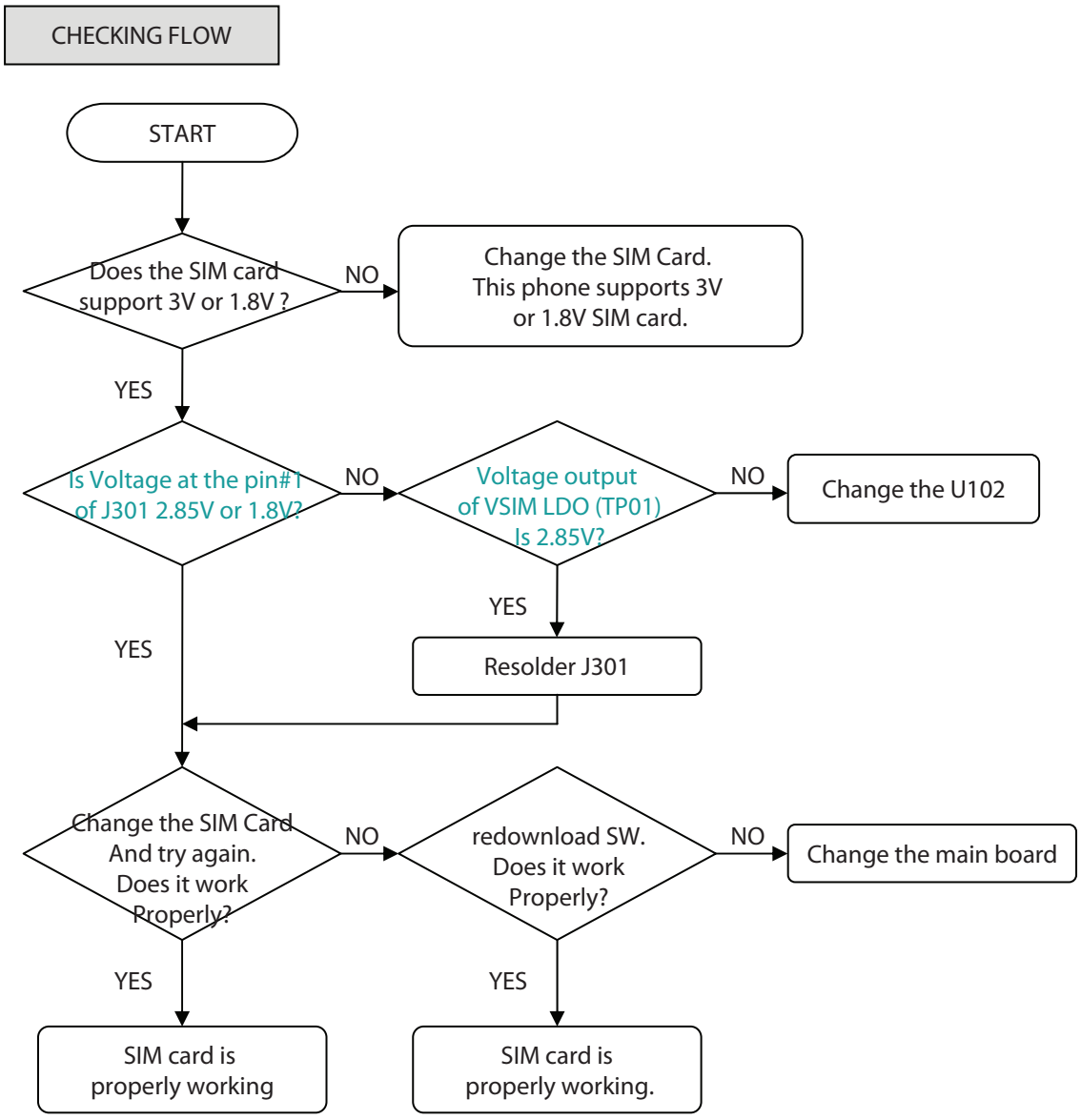


Figure 4.13

CIRCUIT





4.13 Micro SD (uSD) Trouble

TEST POINT

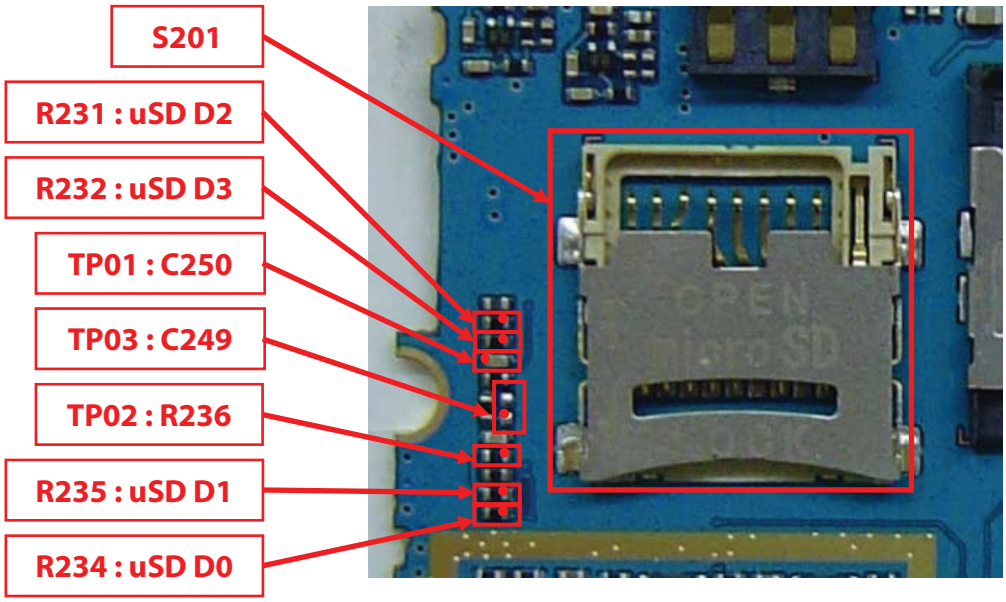
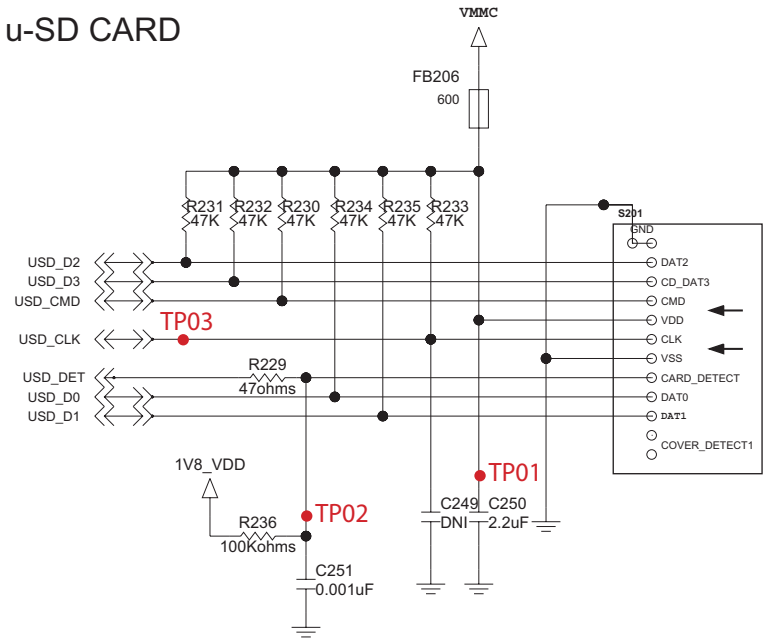
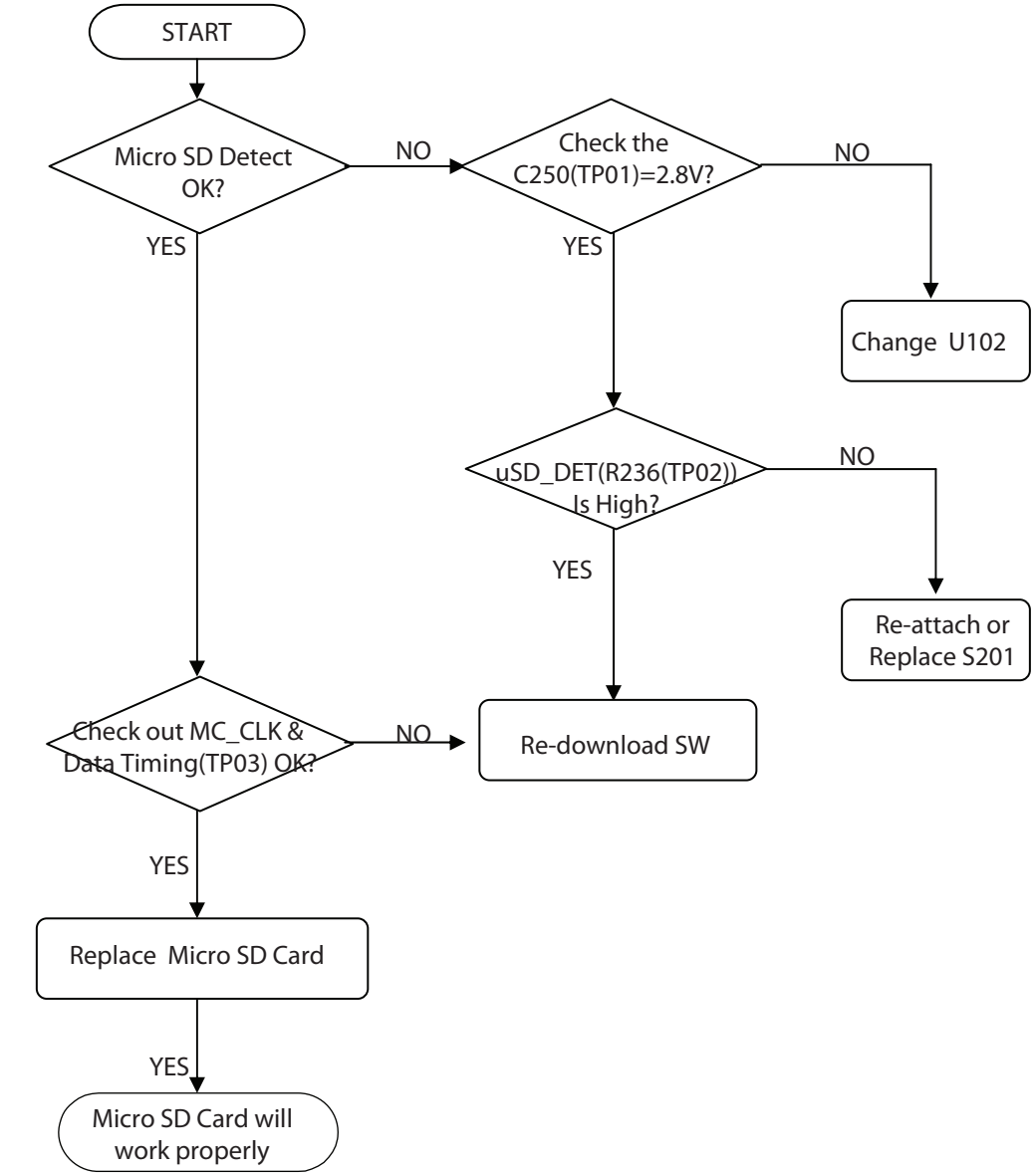


Figure 4.14

CIRCUIT



CHECKING FLOW



4.14 Bluetooth Trouble

Checking Points

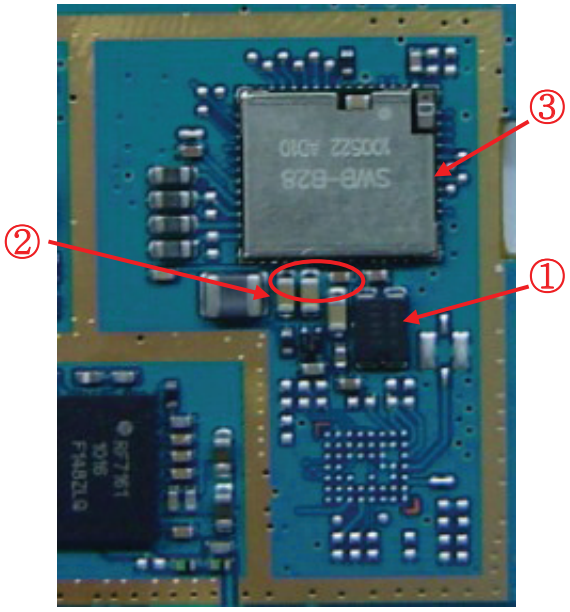
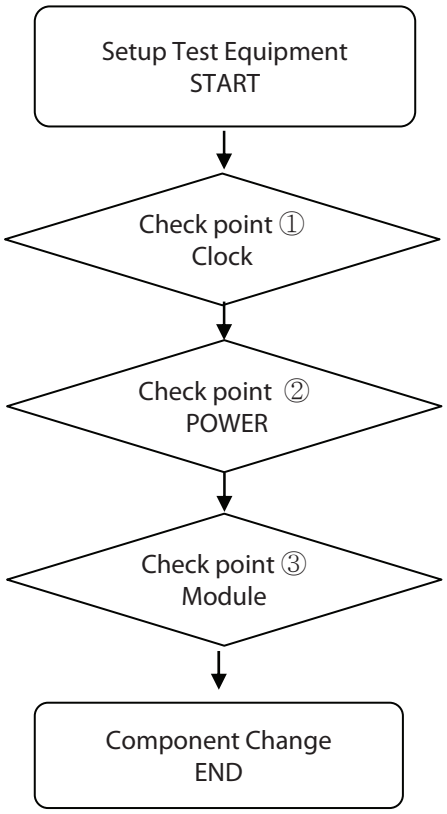


Figure 4-14. WI-FI/BT Module

Checking Flow



4.14.1 Checking Main Clock part

Checking Points

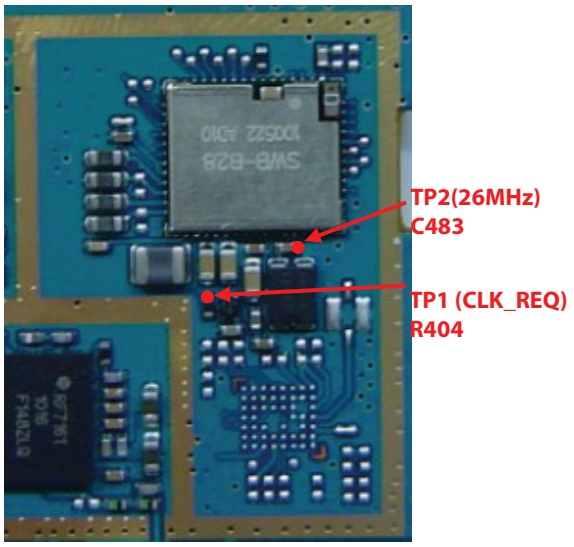
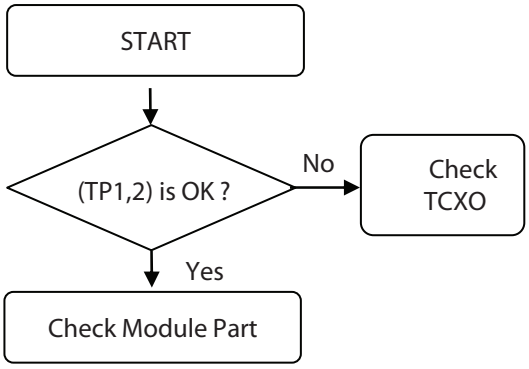


Figure 4-16-1. WI-FI/BT Clock part

Checking Flow



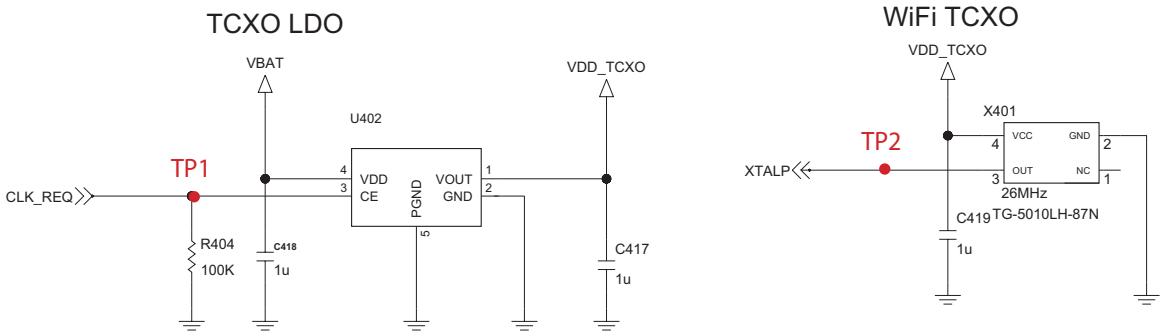
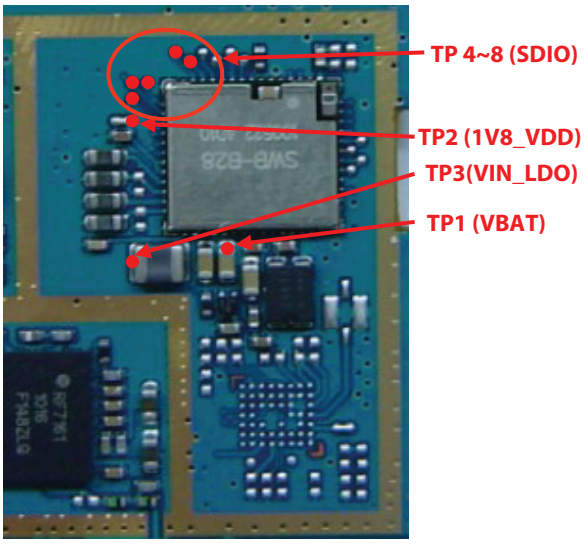


Figure 4-16. WI-FI/BT Clock Circuit

4.14.2. Checking Module Part

Checking Points



Checking Flow

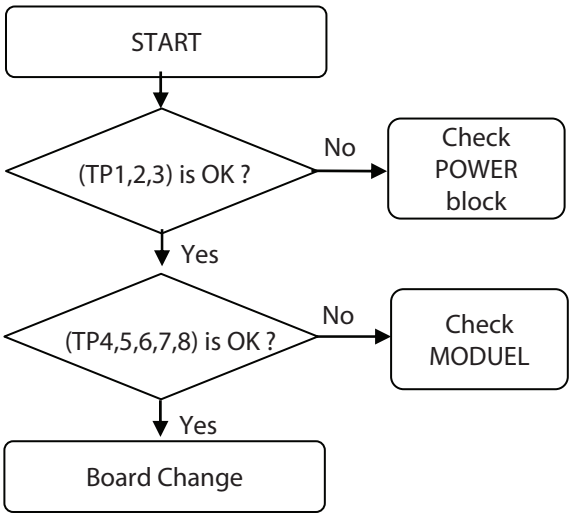


Figure 4-14-2. WI-FI/BT MODULE

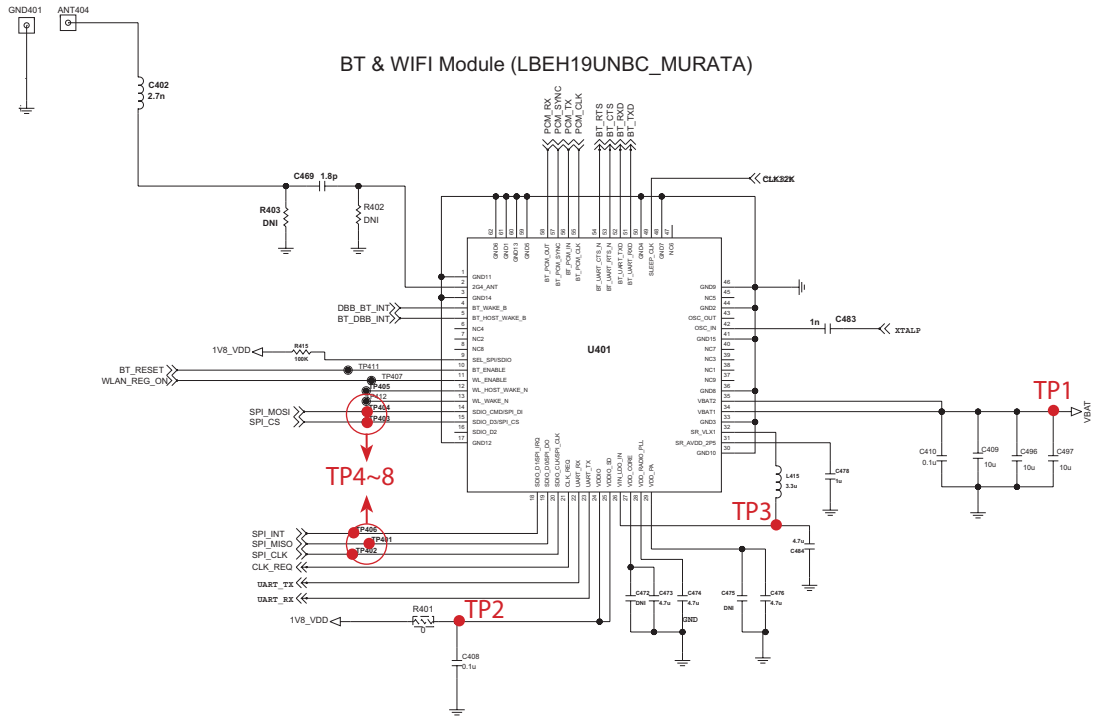


Figure 4-14-3. WI-FI/BT MODULE Circuit

4.15 FM Radio Trouble

TEST POINT

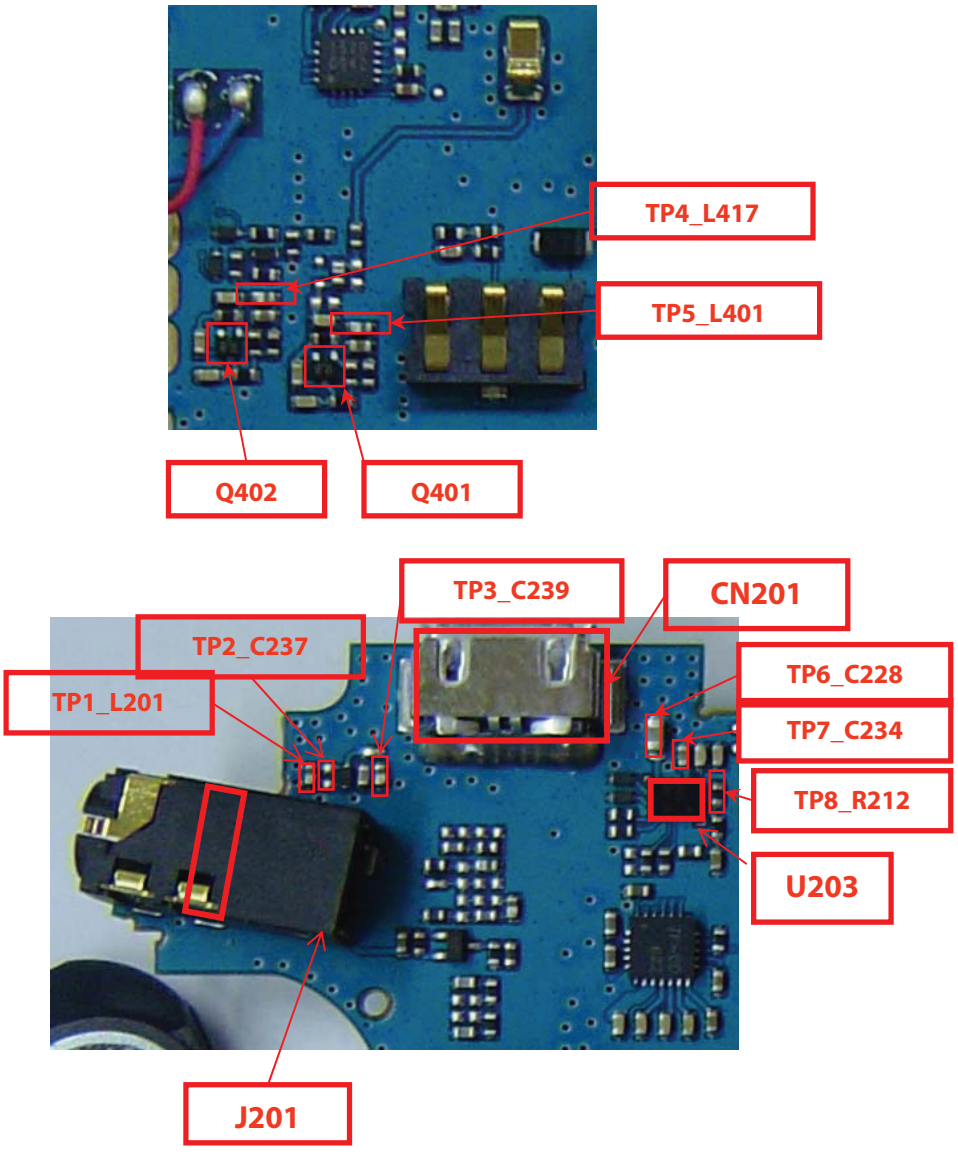
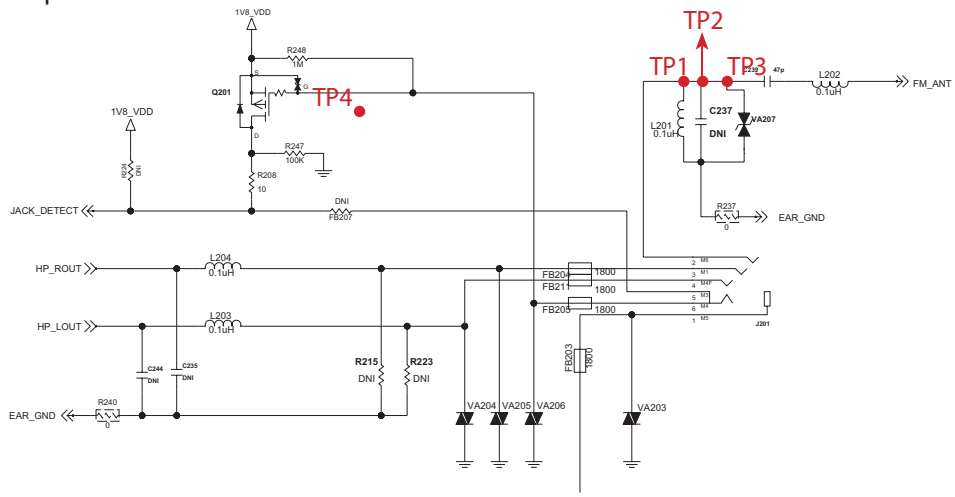


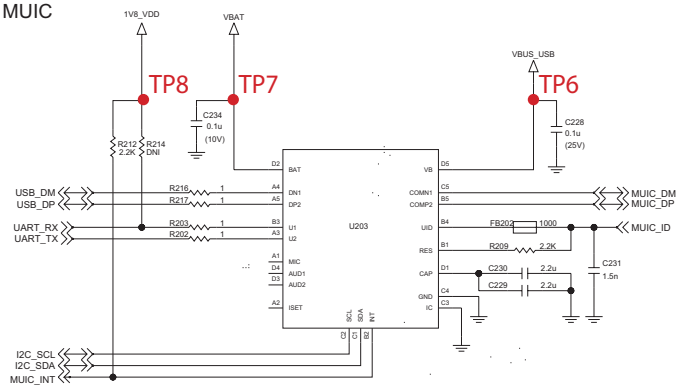
Figure 4.17

CIRCUIT

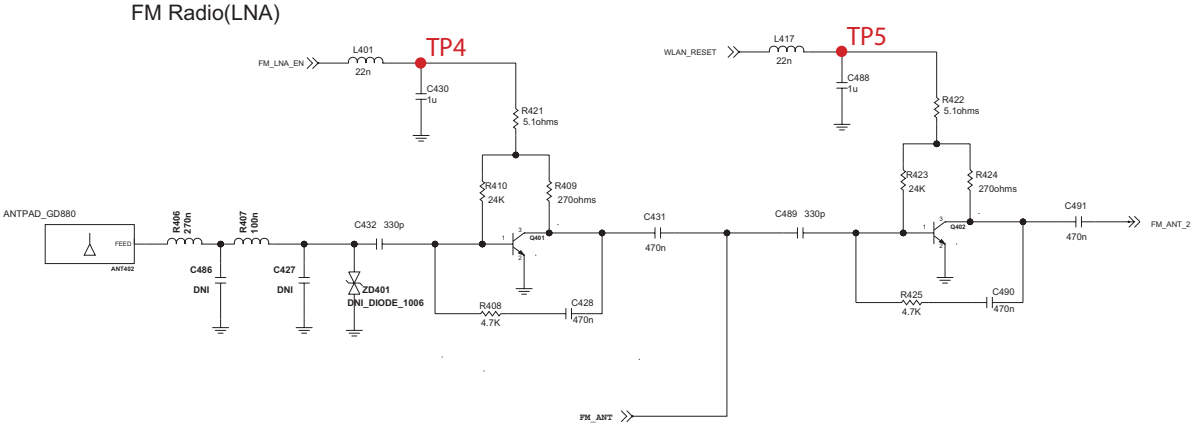
3.5phi HEADSET



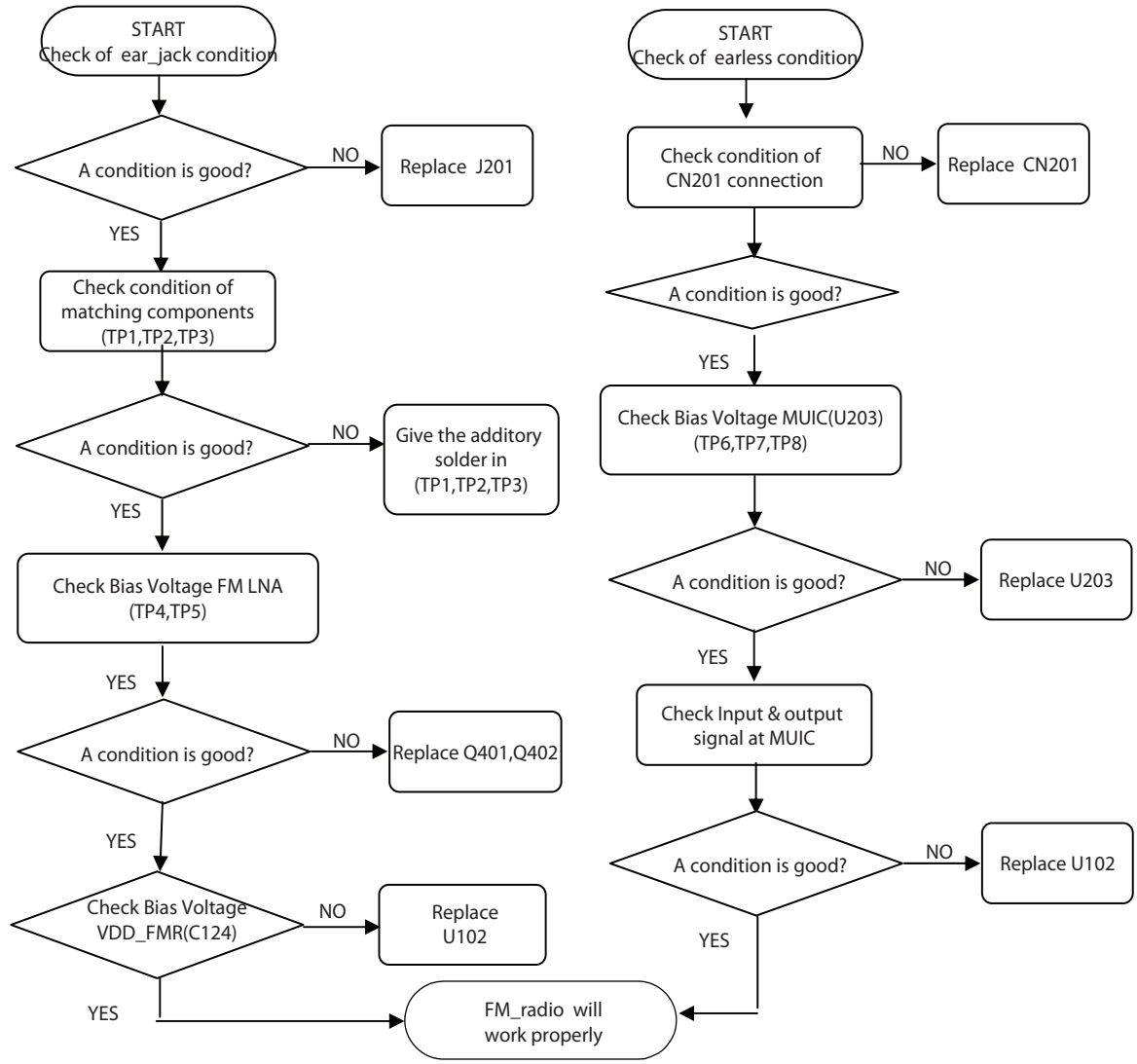
MUIC



FM Radio(LNA)

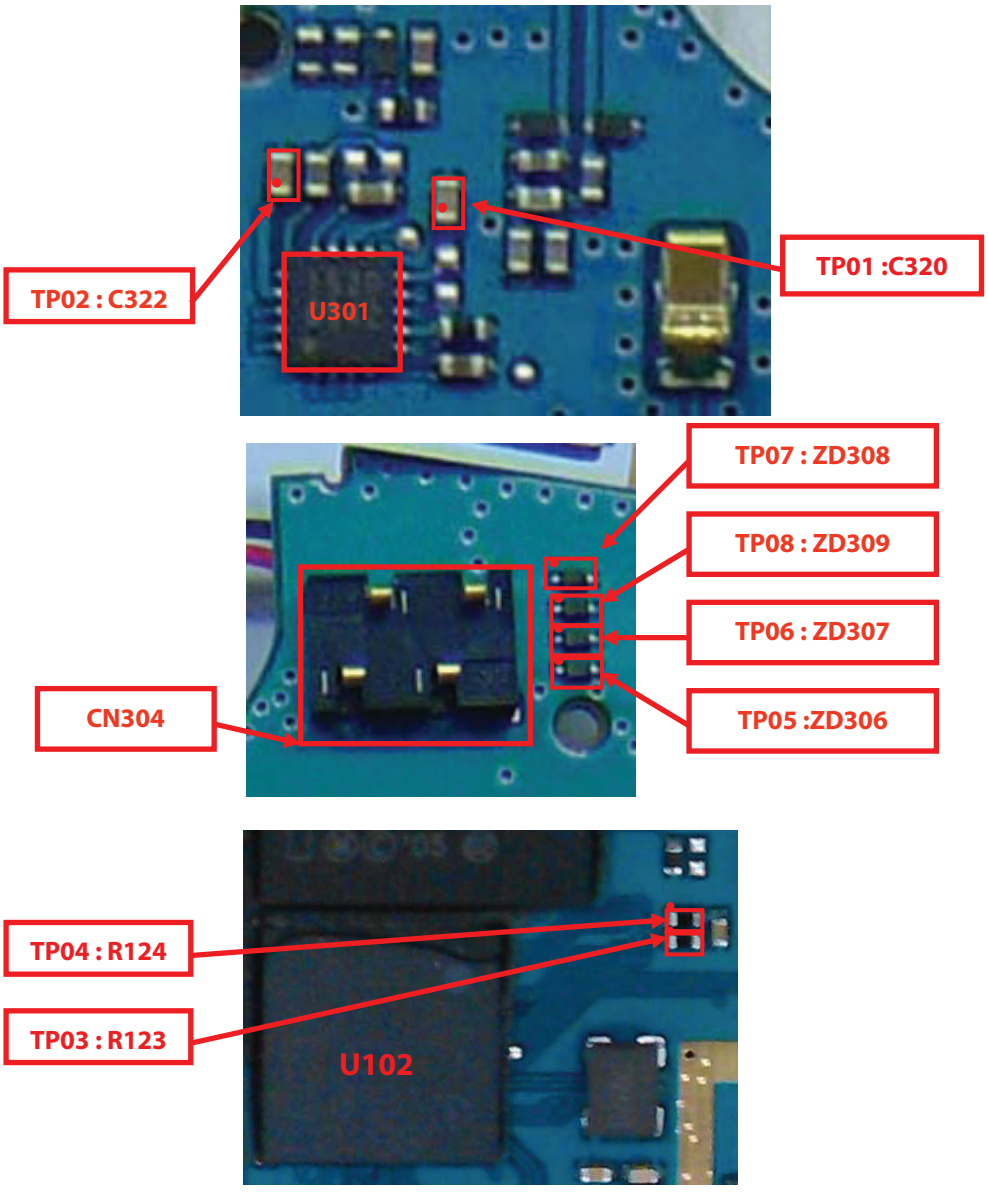


CHECKING FLOW

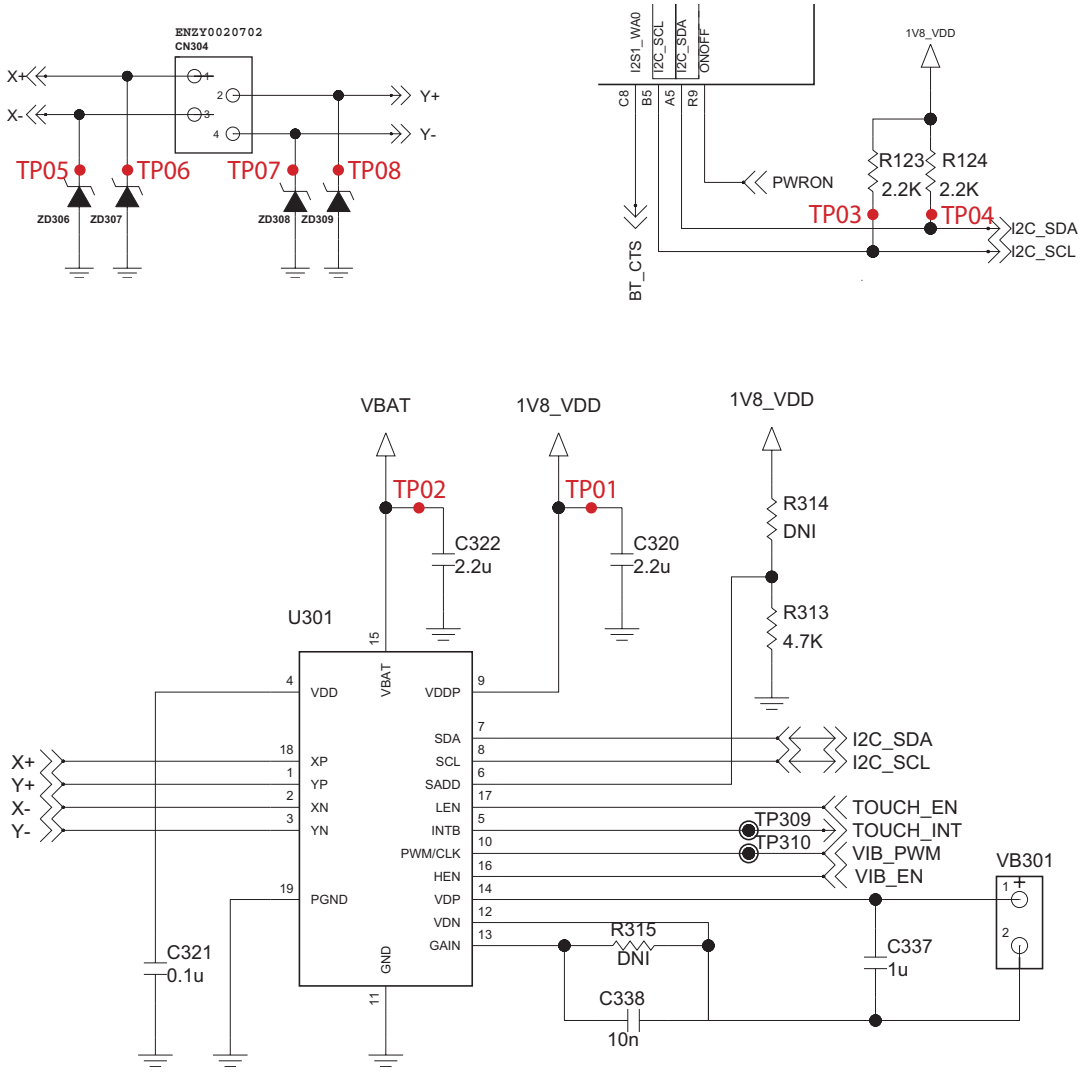


4.16 Touch trouble

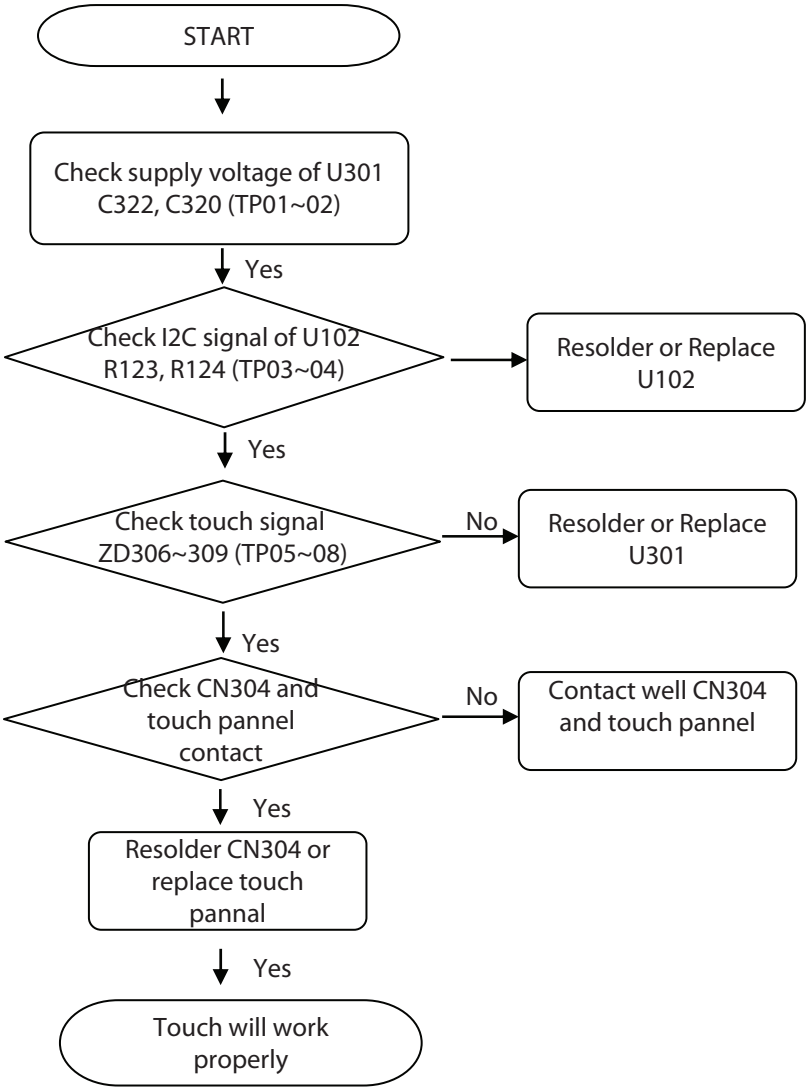
TEST POINT



CIRCUIT



CHECKING FLOW



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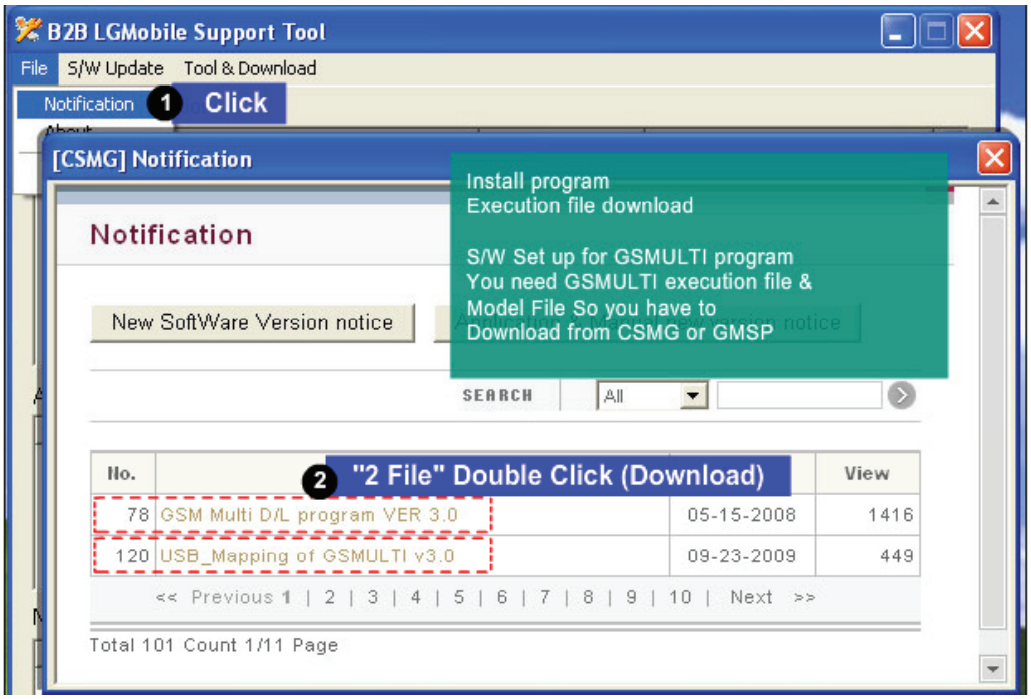

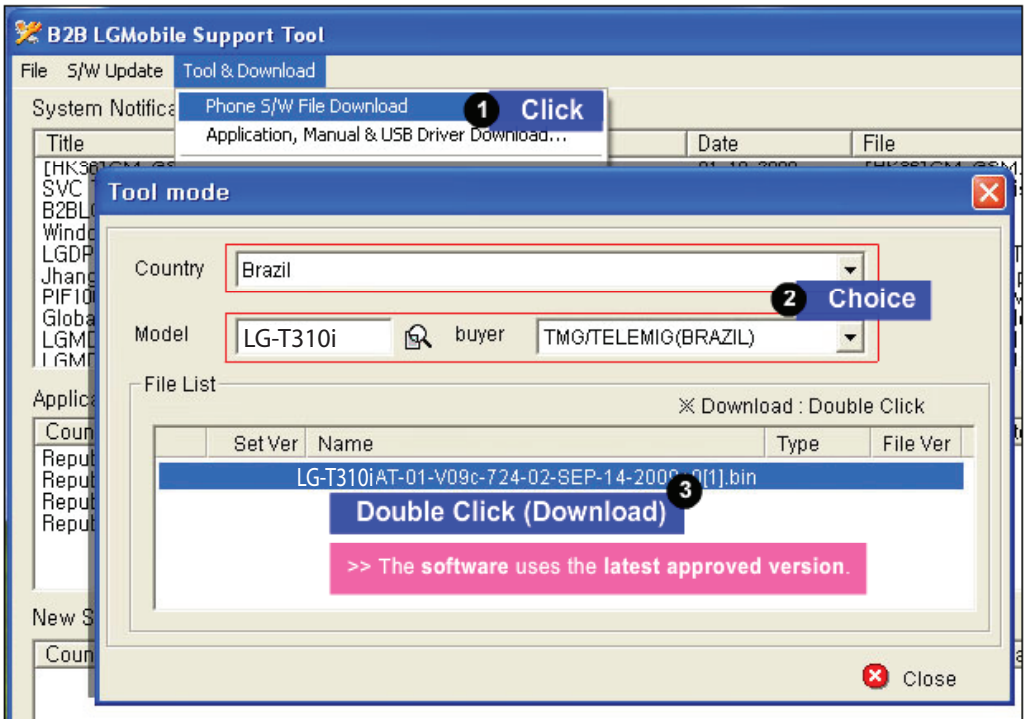

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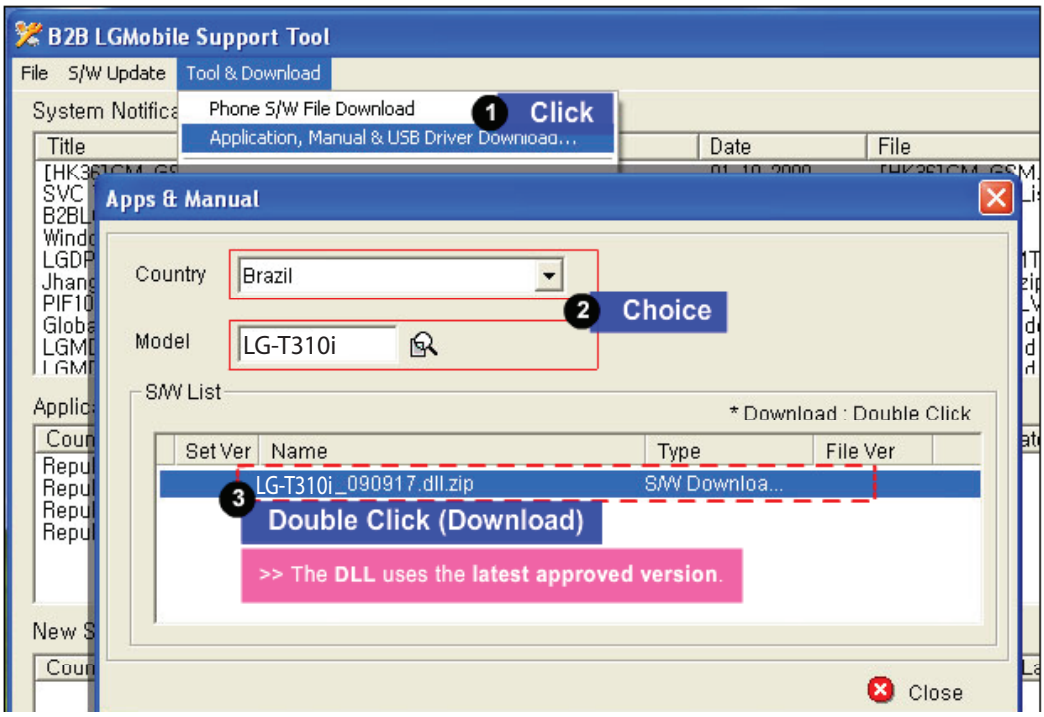

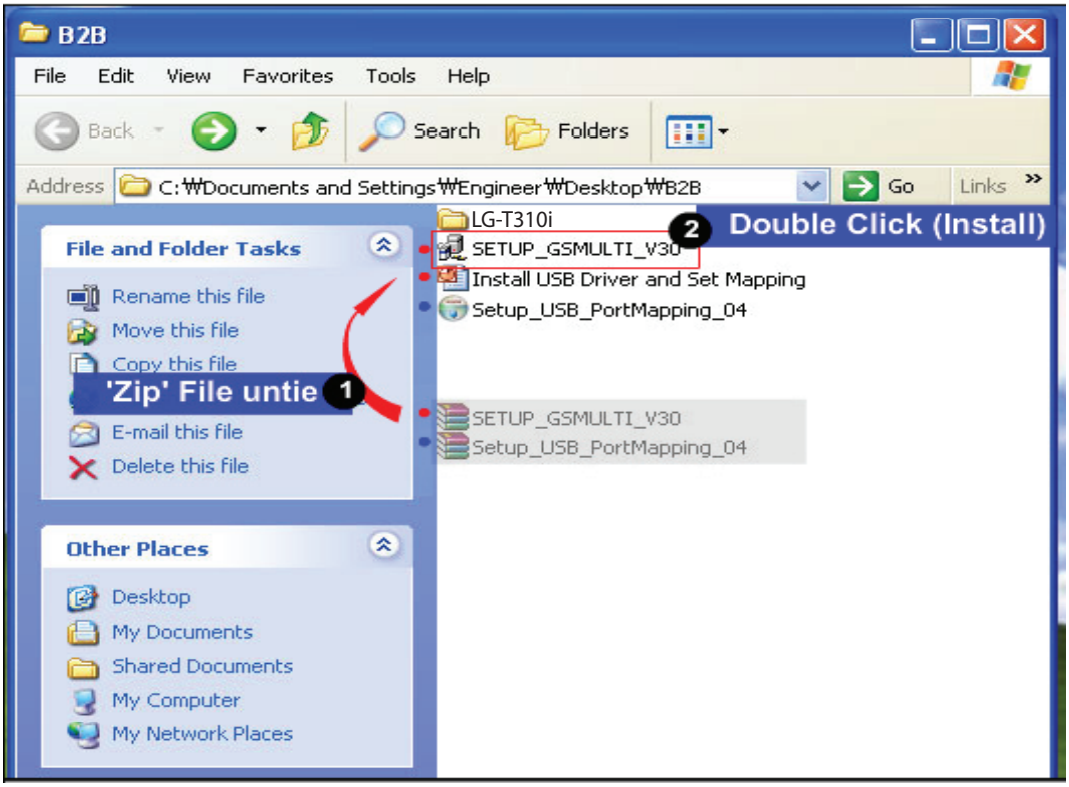

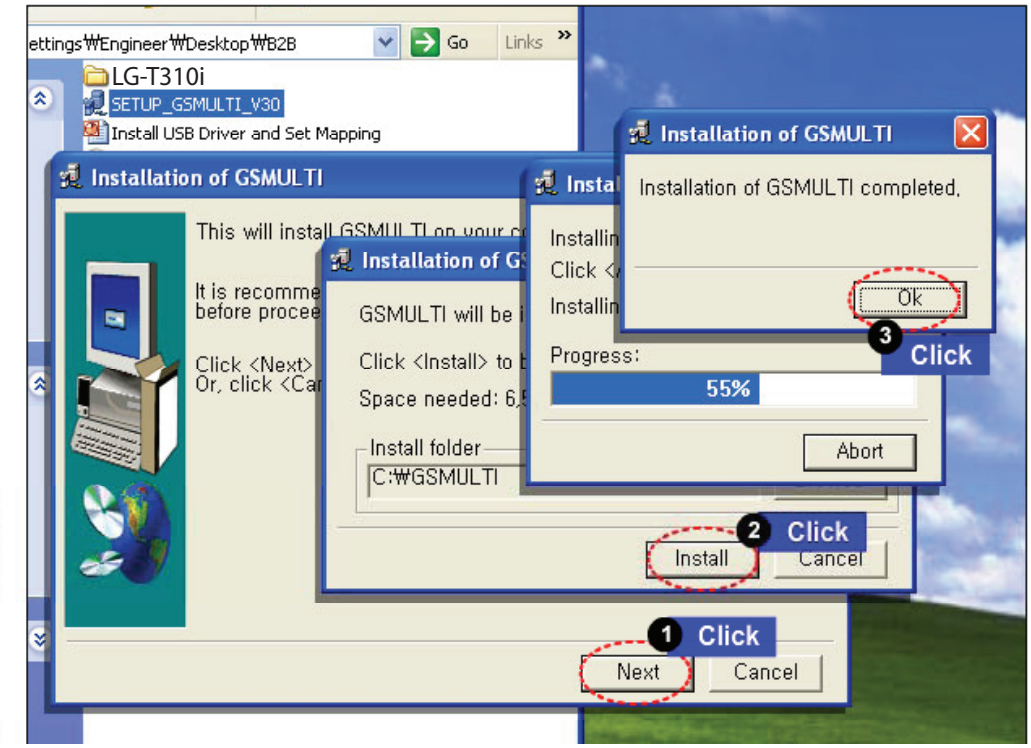

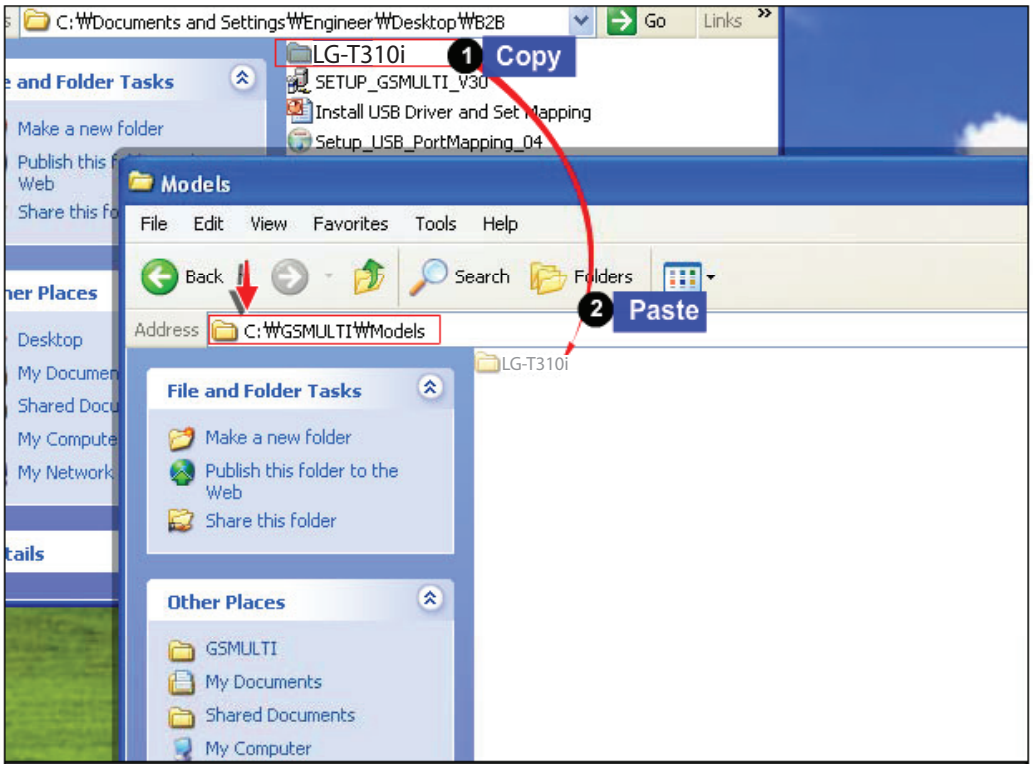

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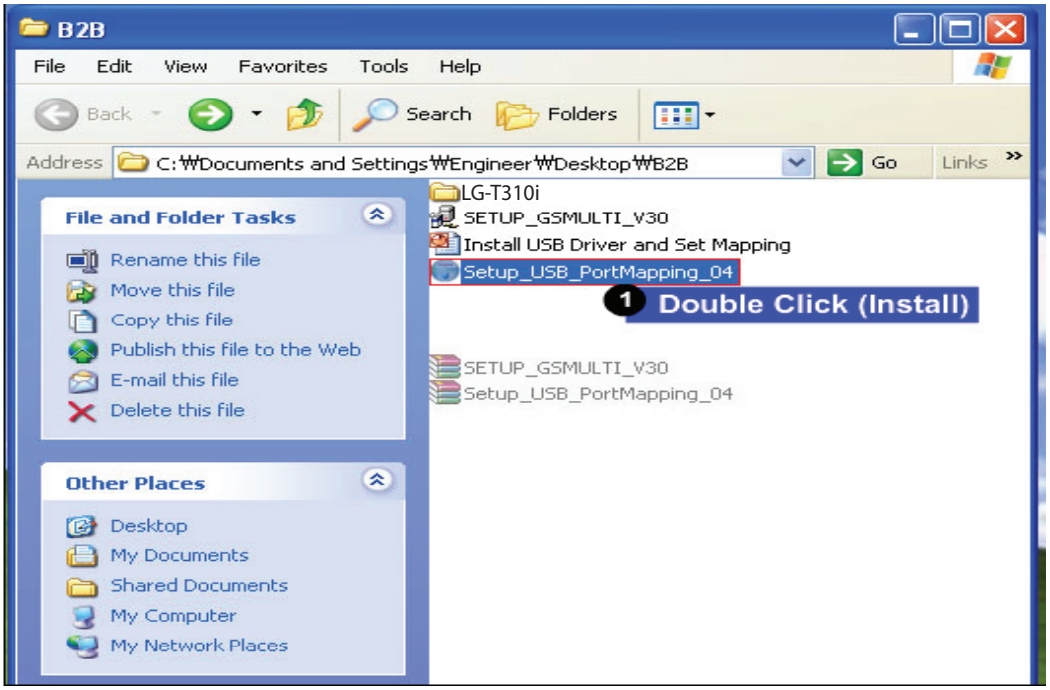

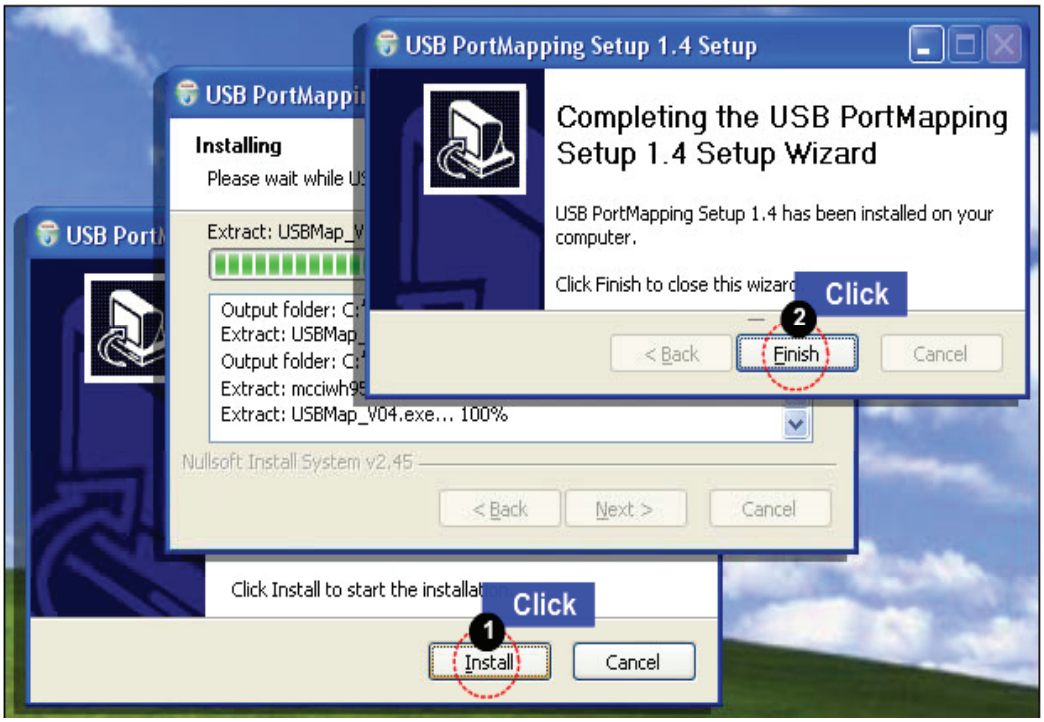

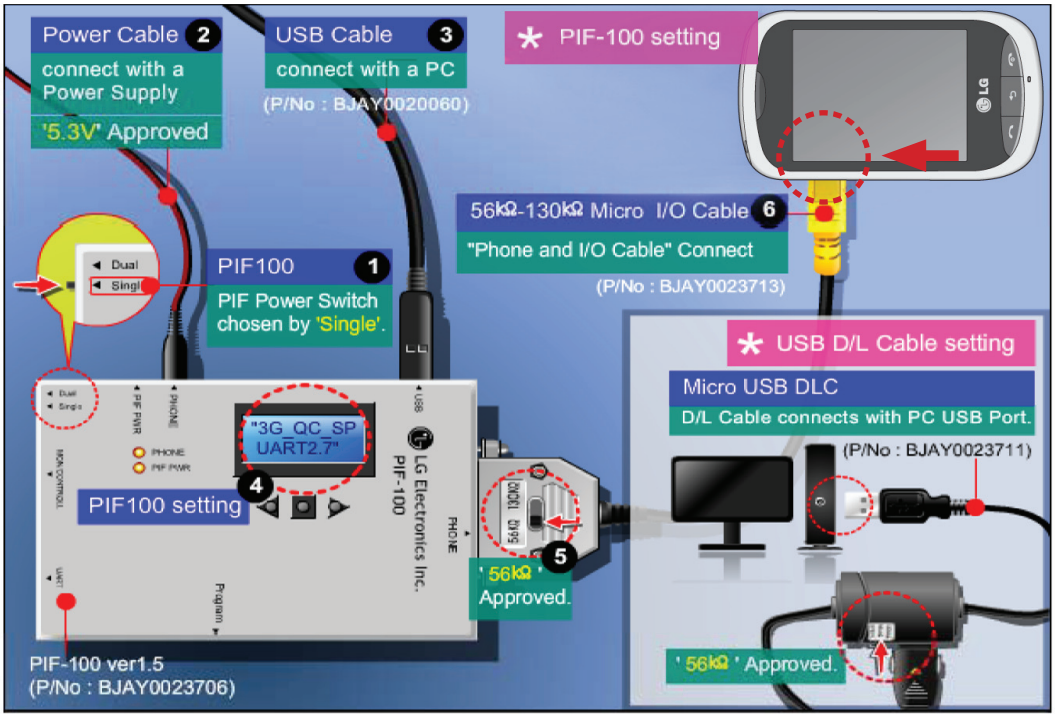

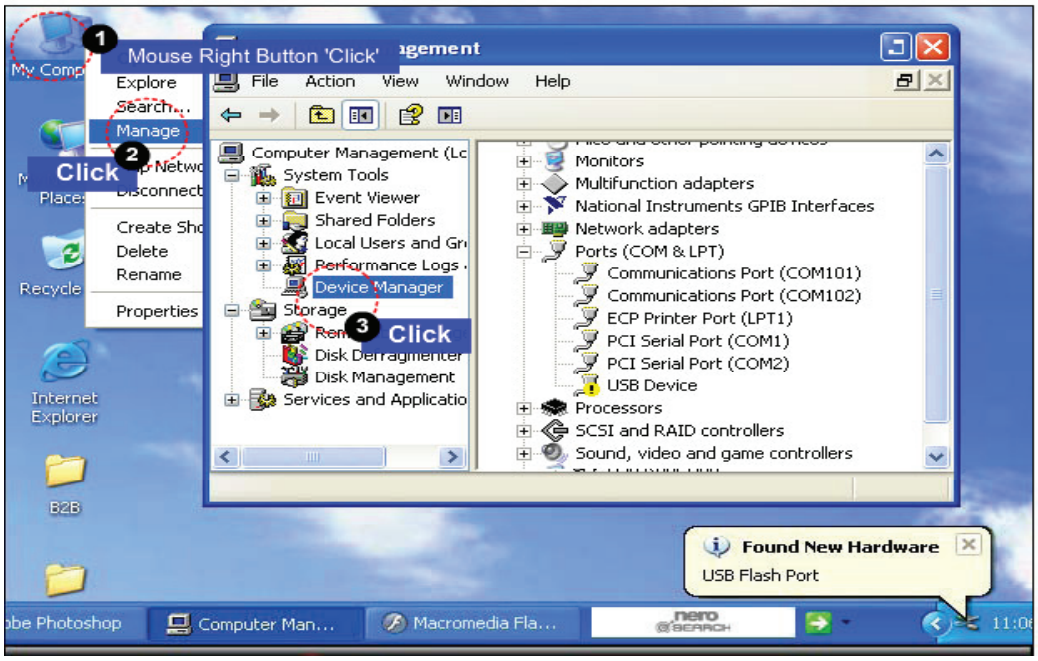

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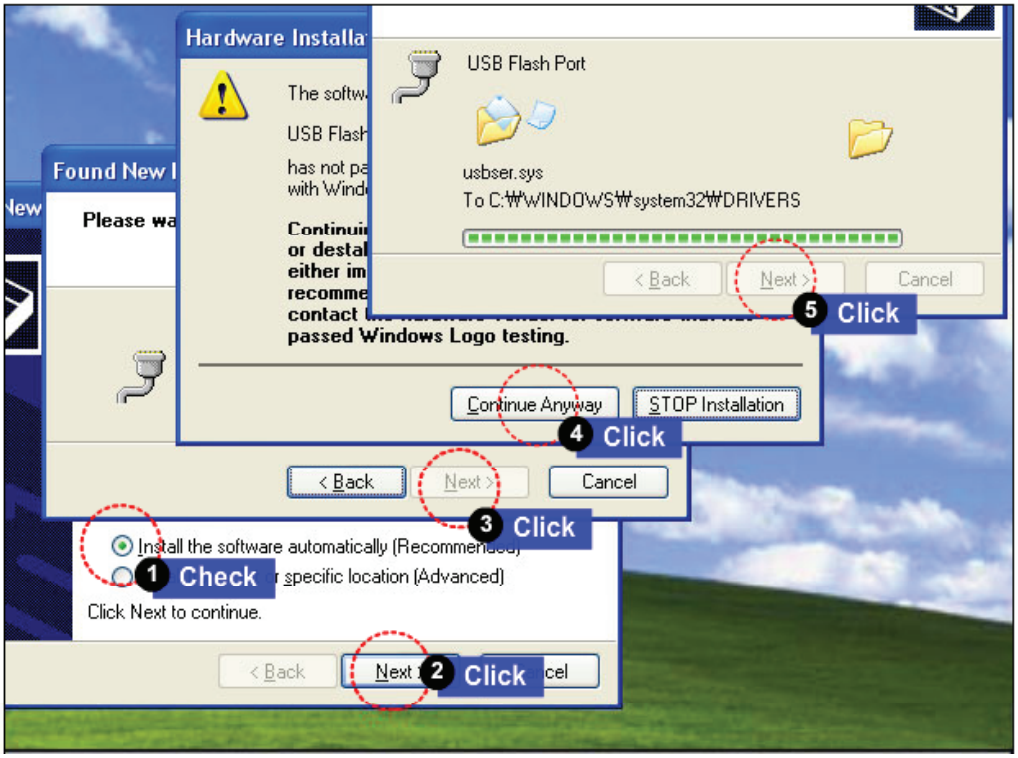

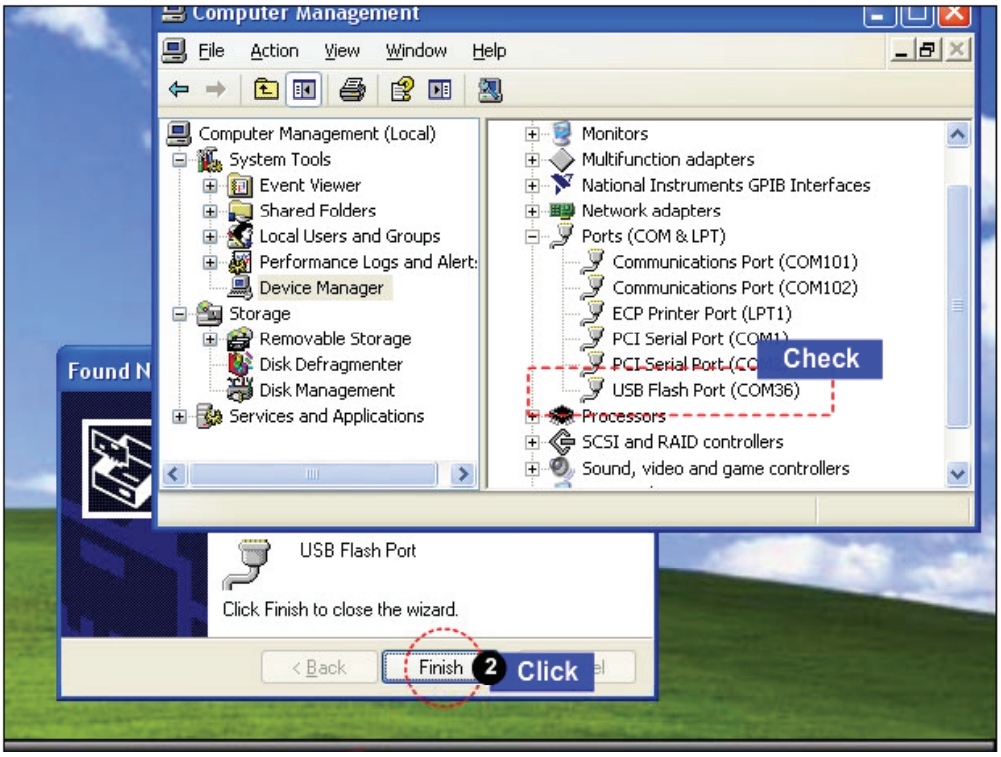

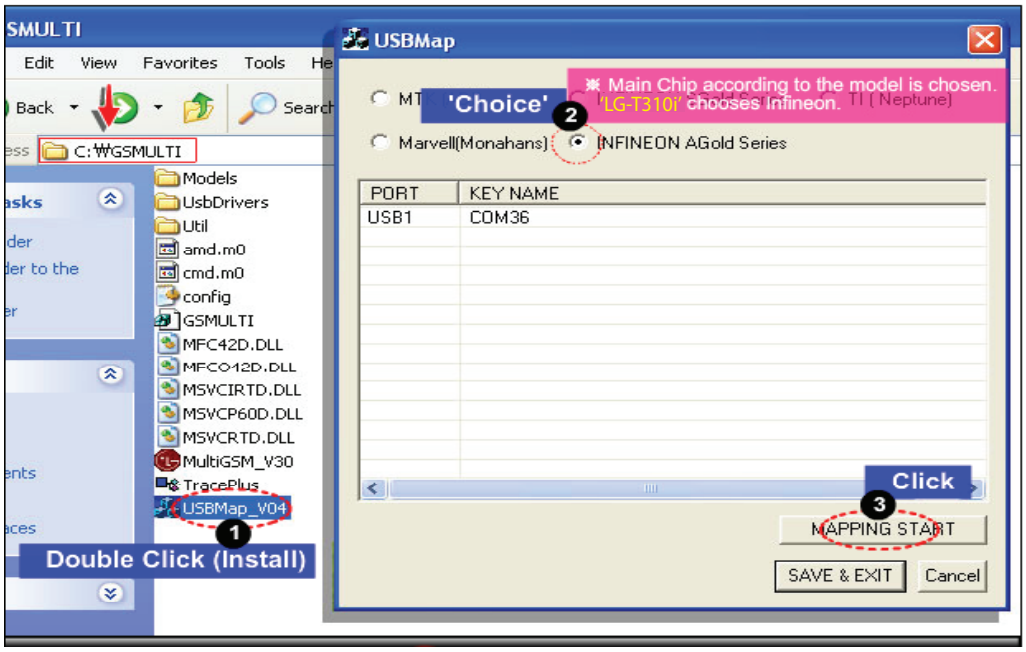

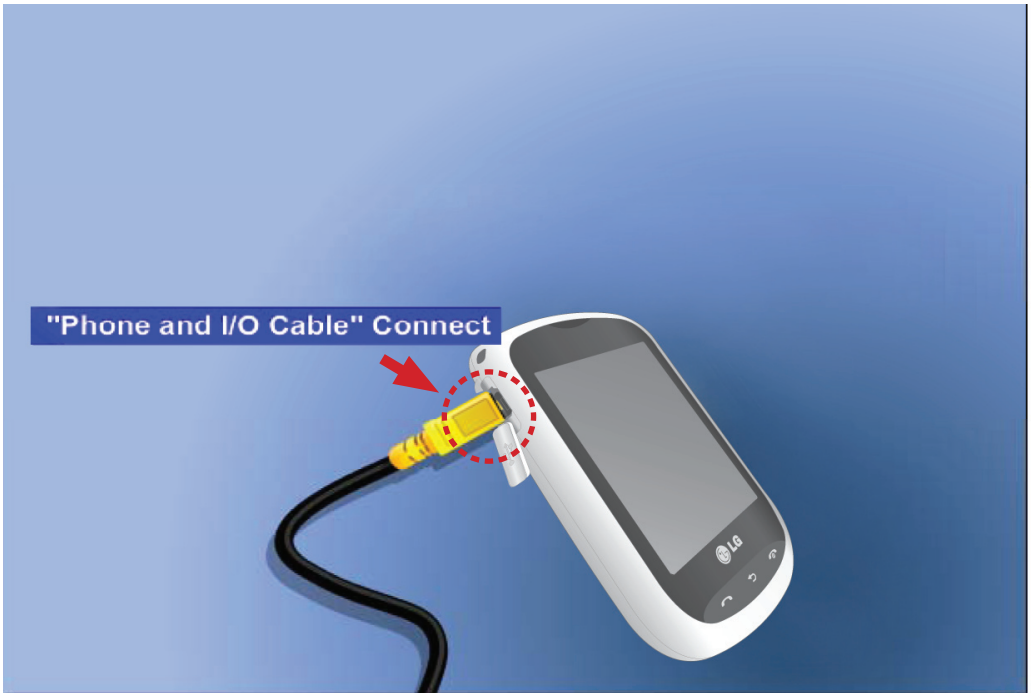

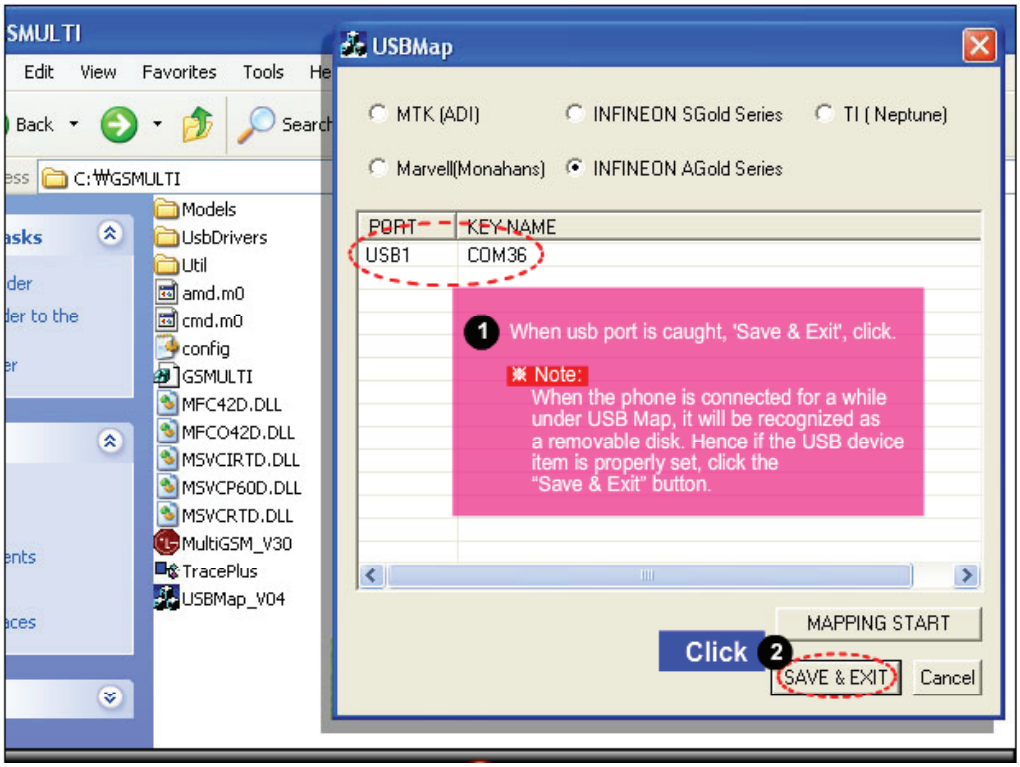

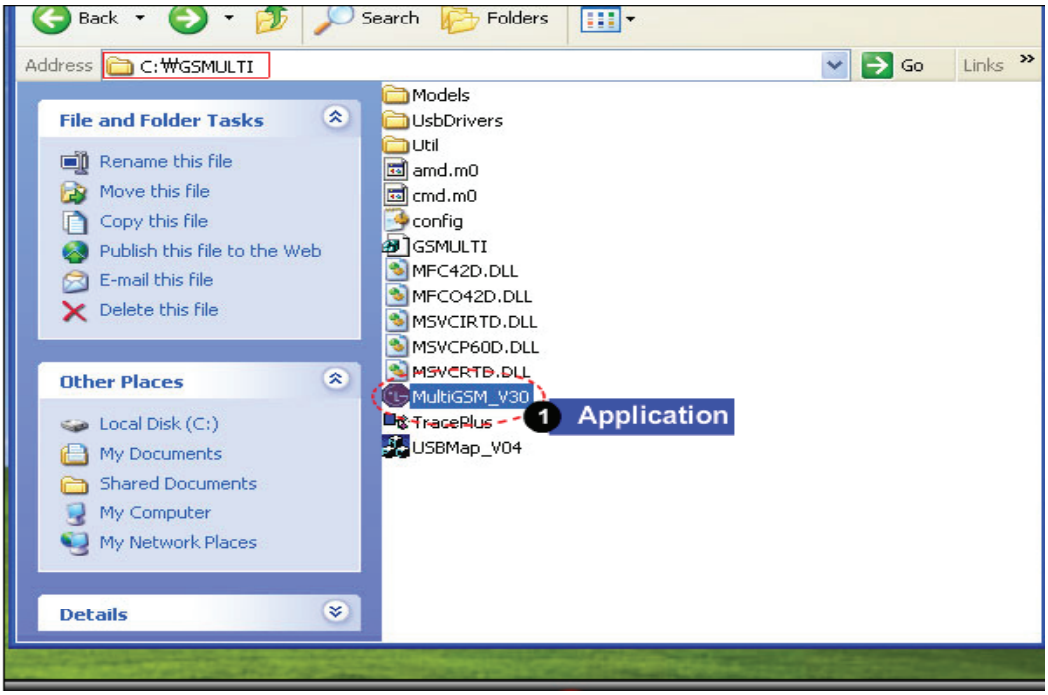

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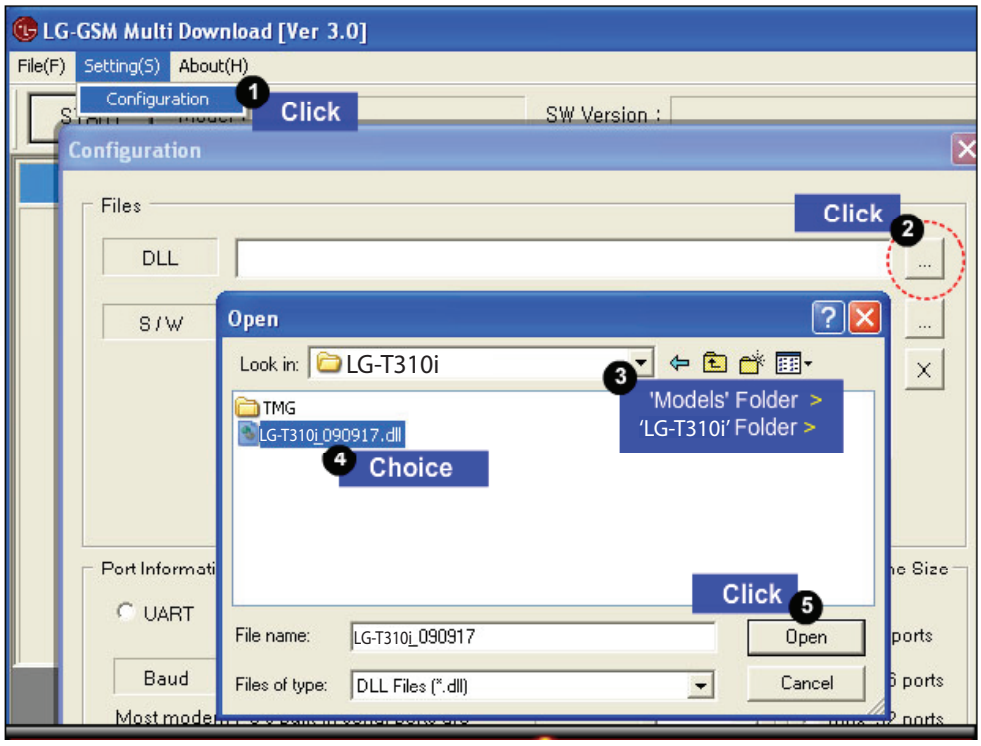
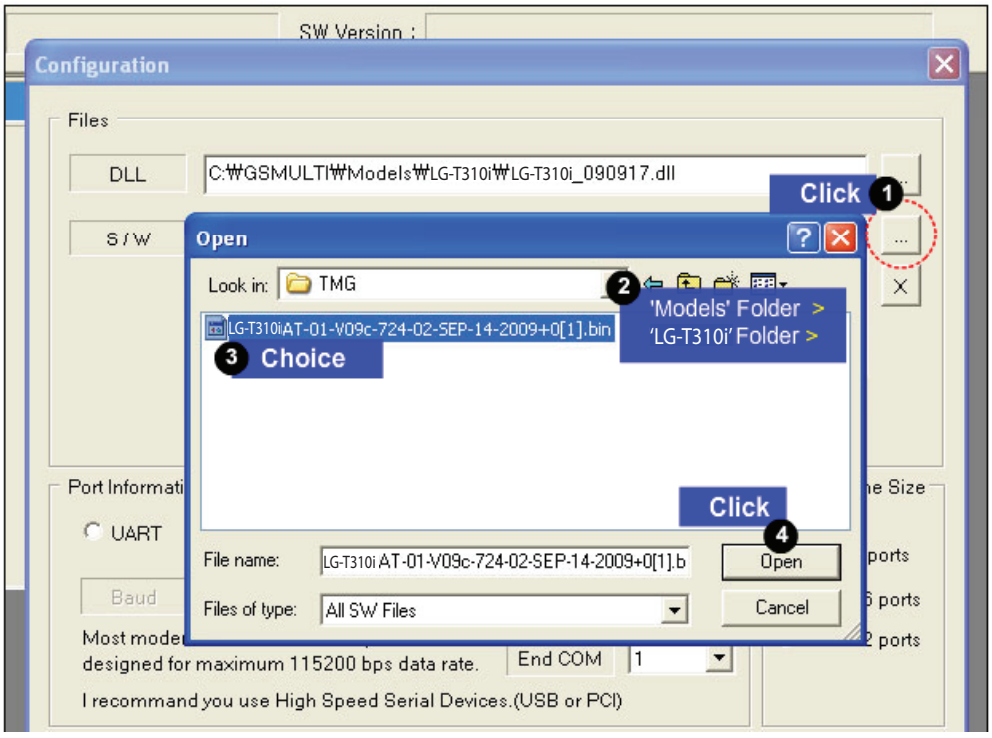
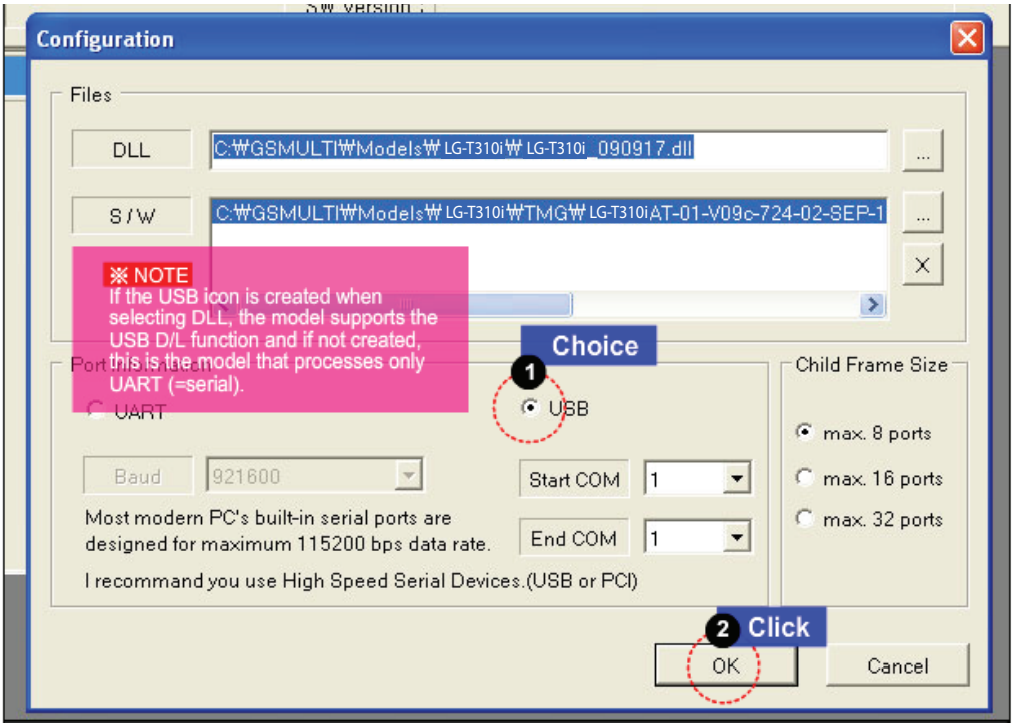
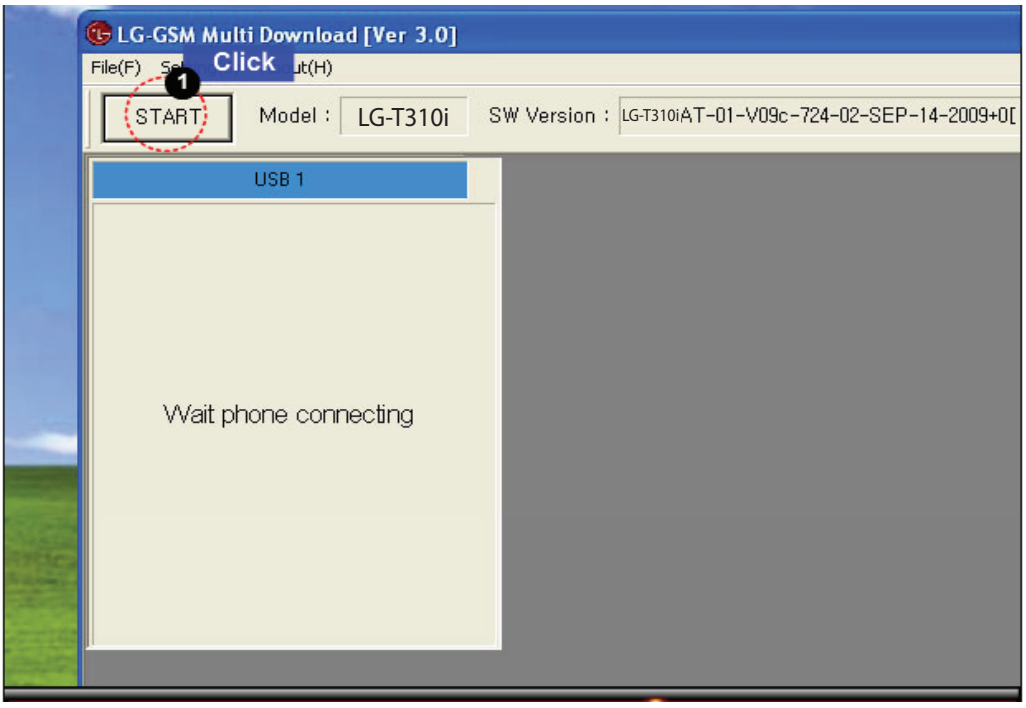
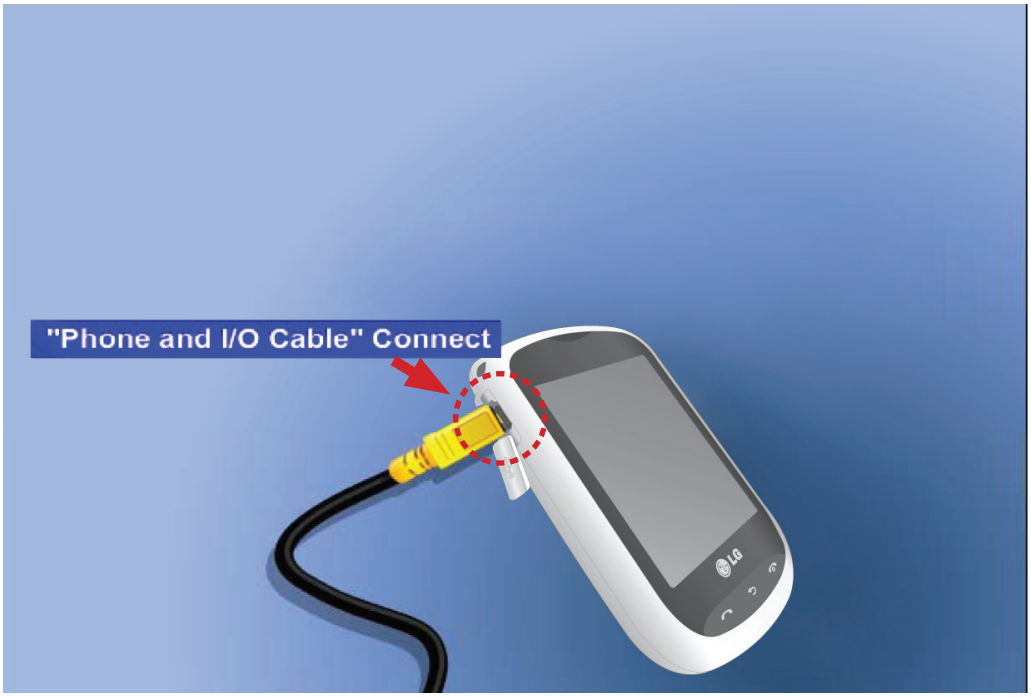
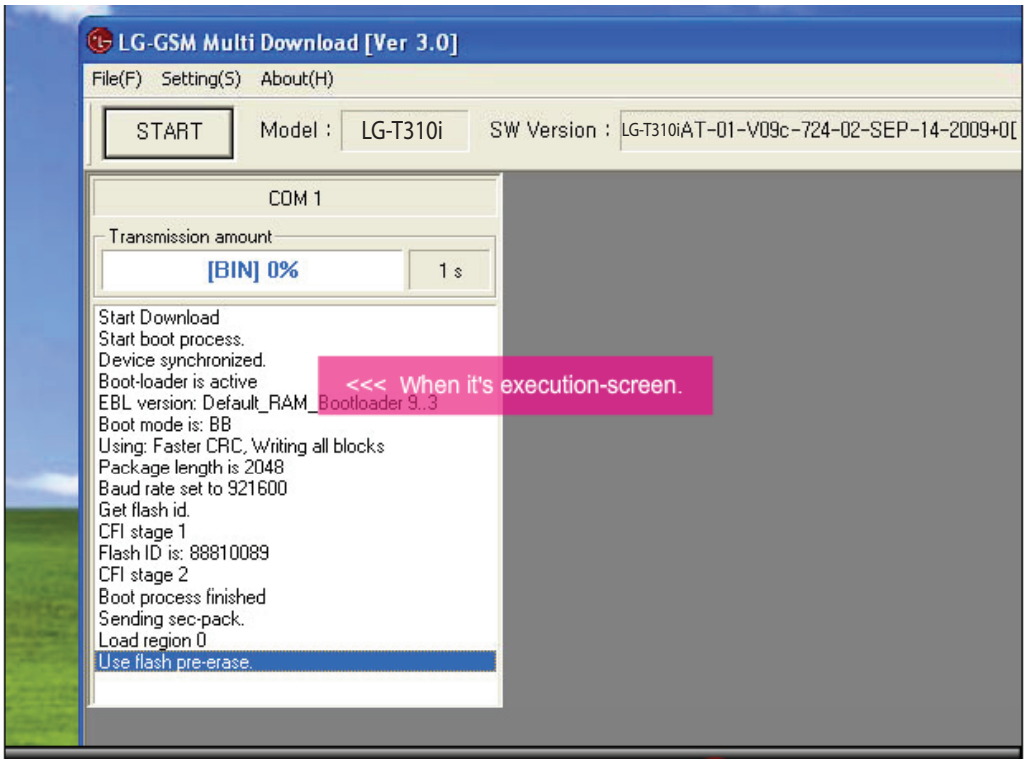


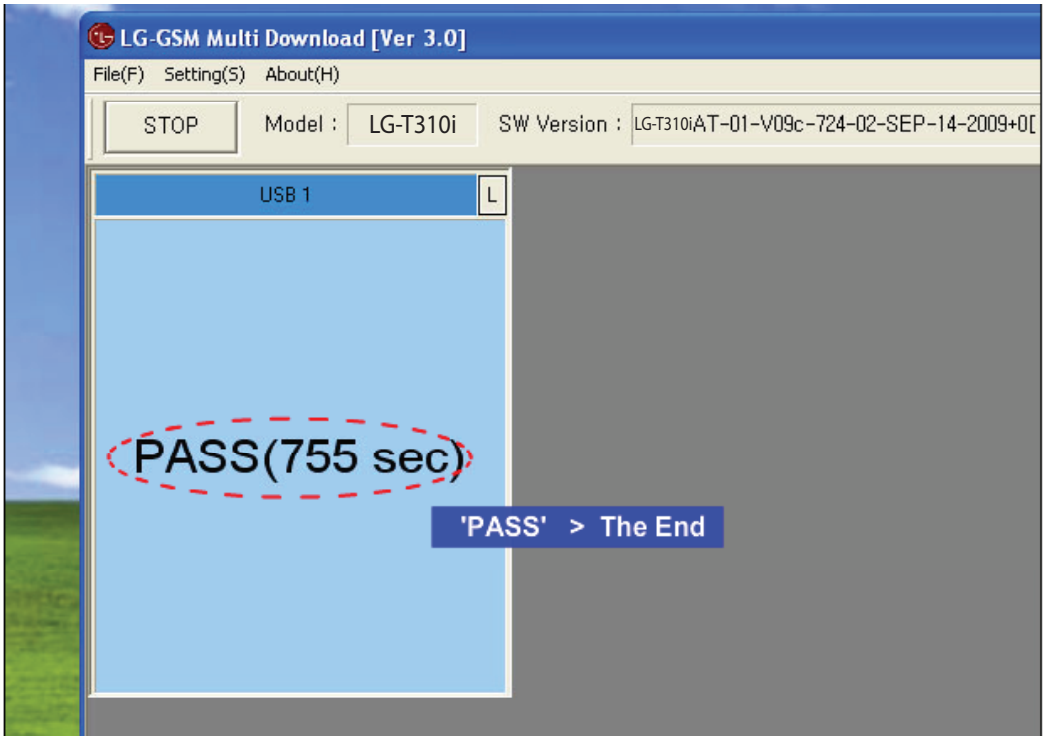




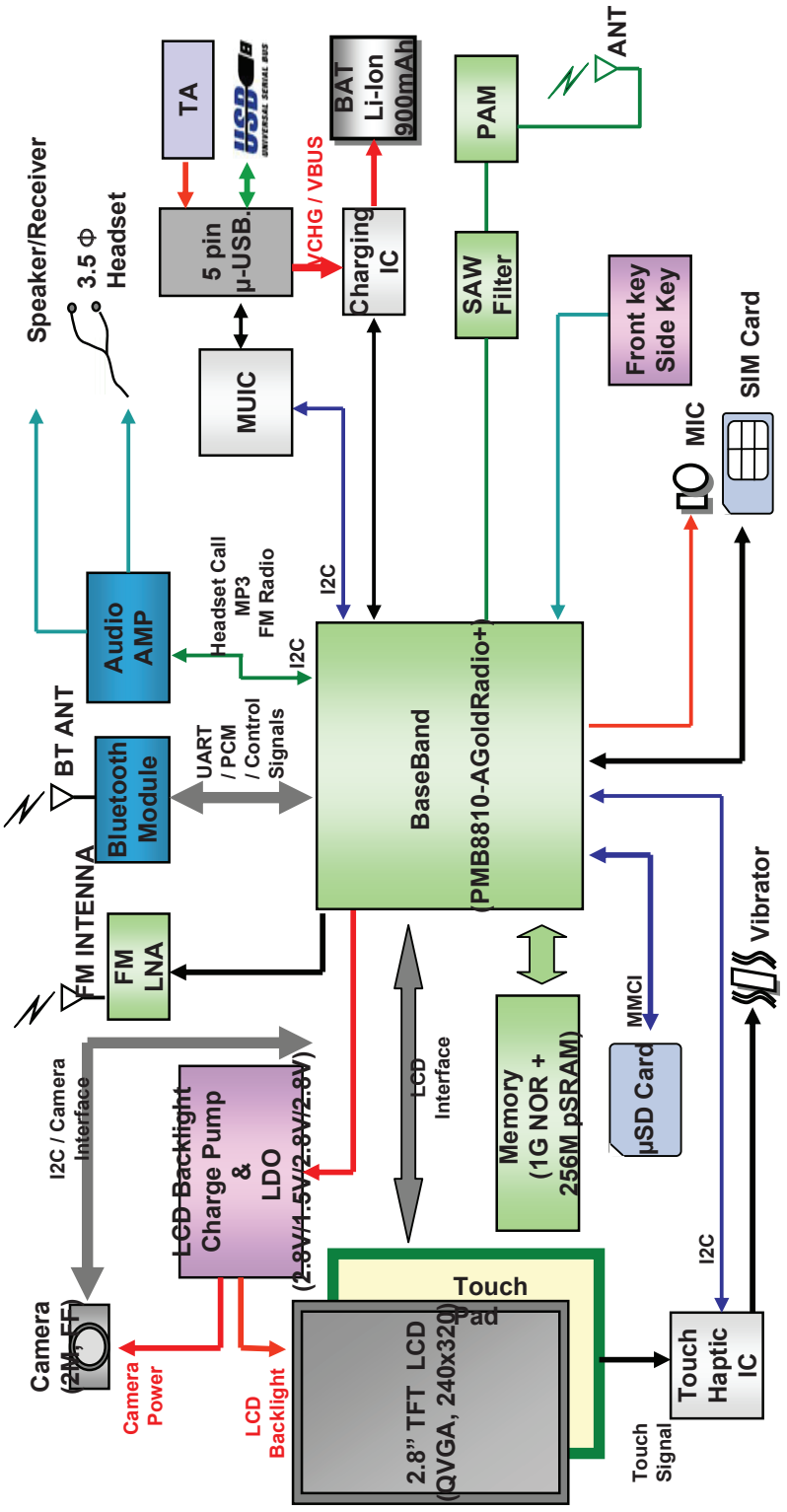




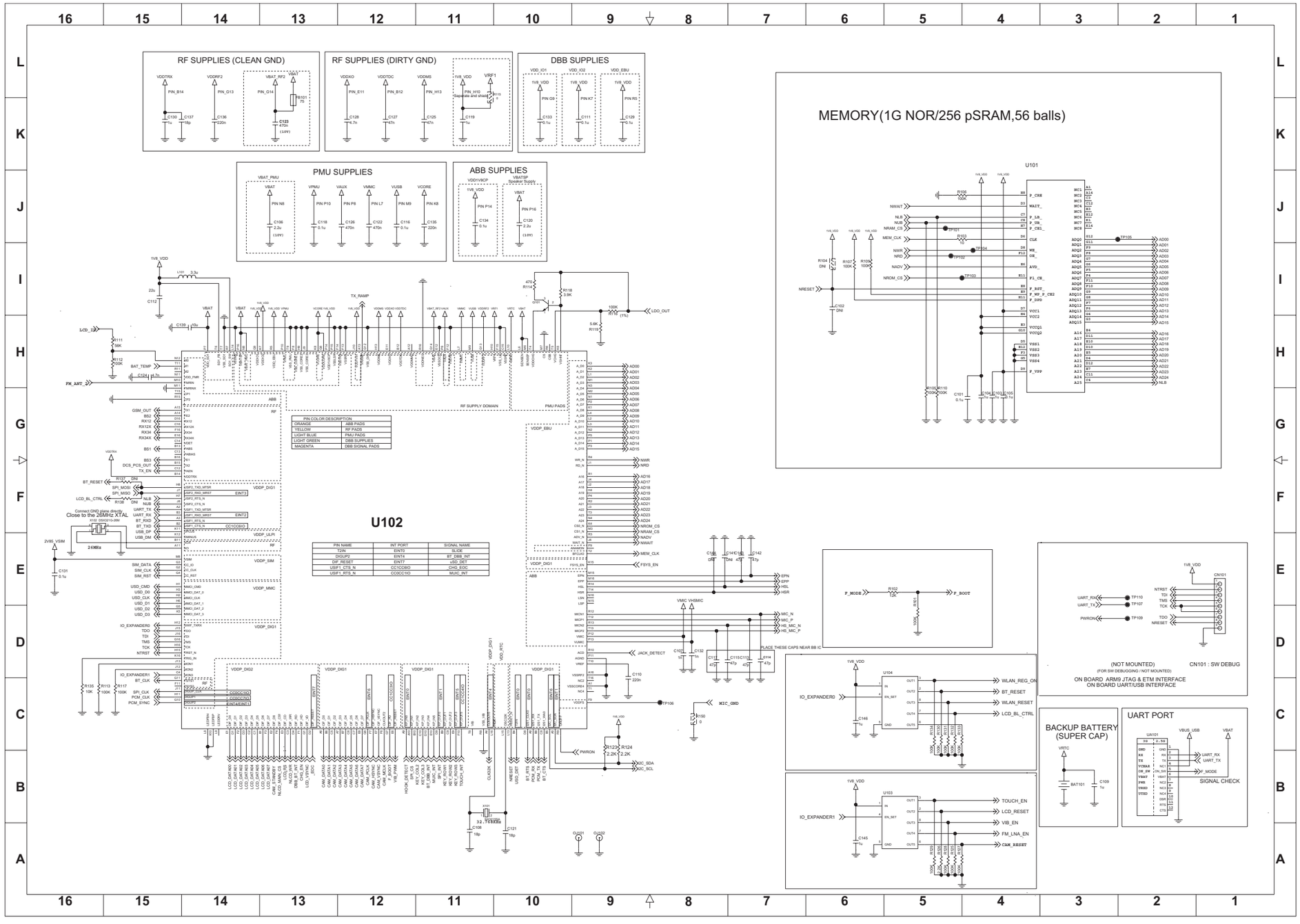




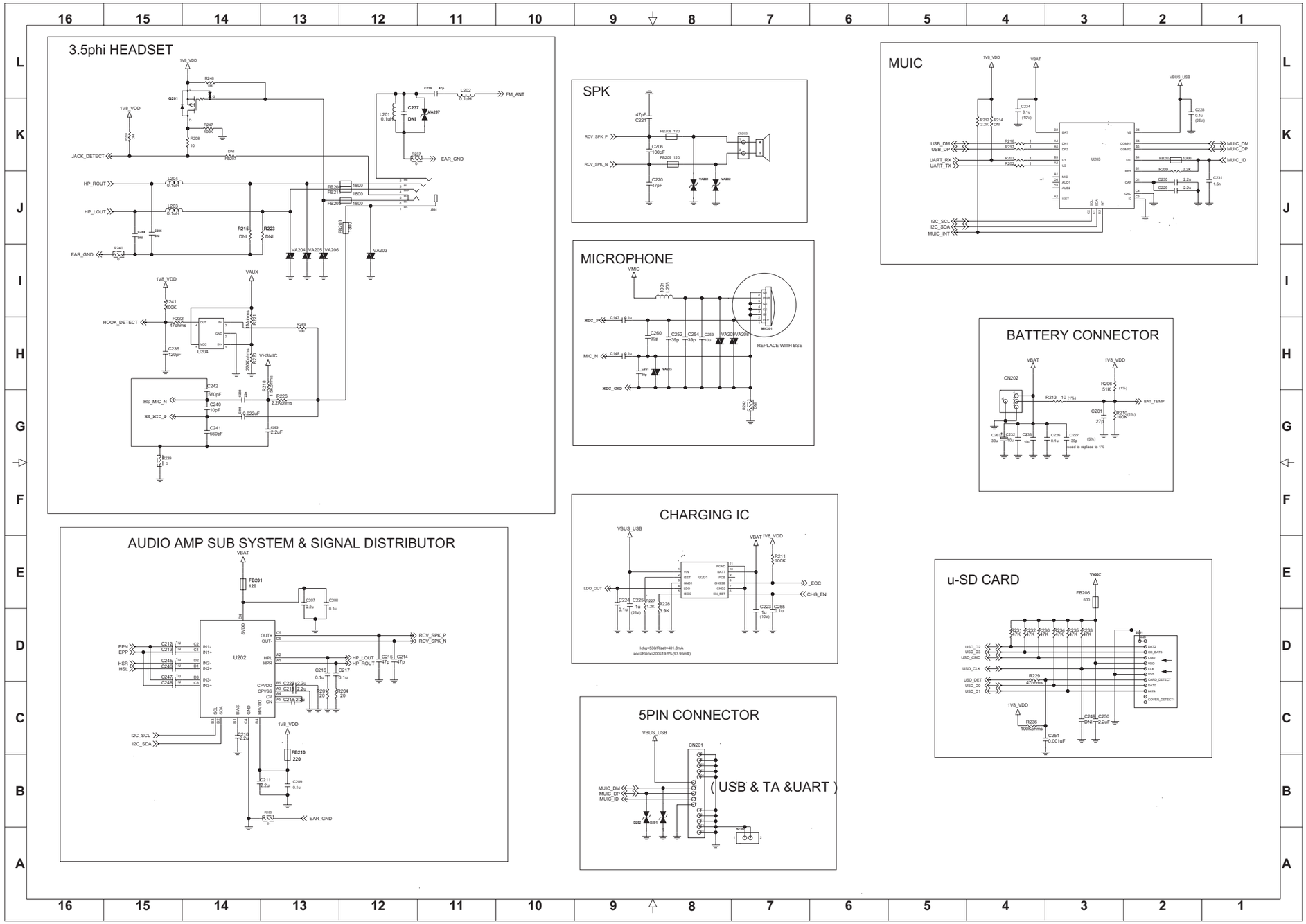
6. BLOCK DIAGRAM



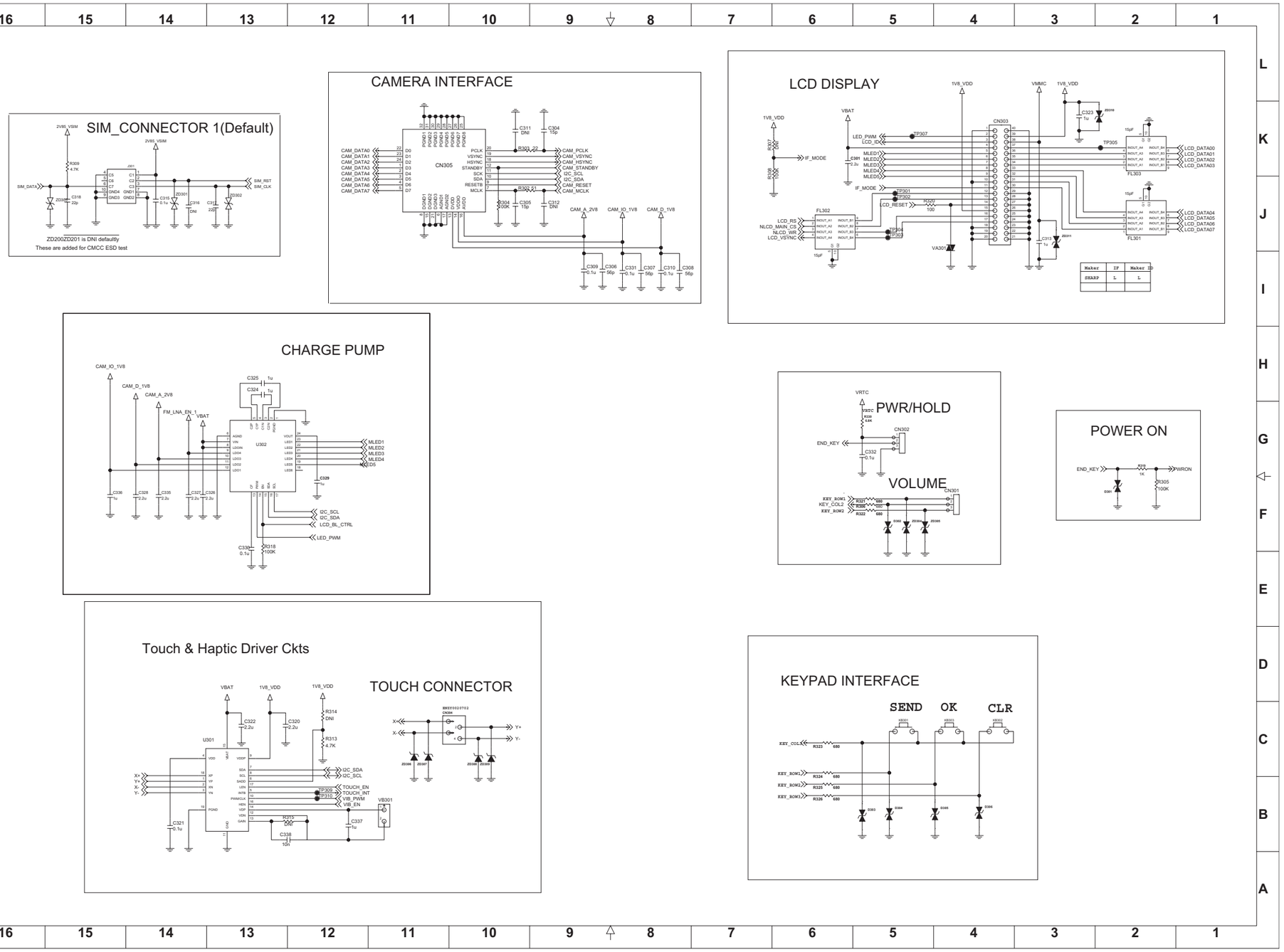
7. CIRCUIT DIAGRAM



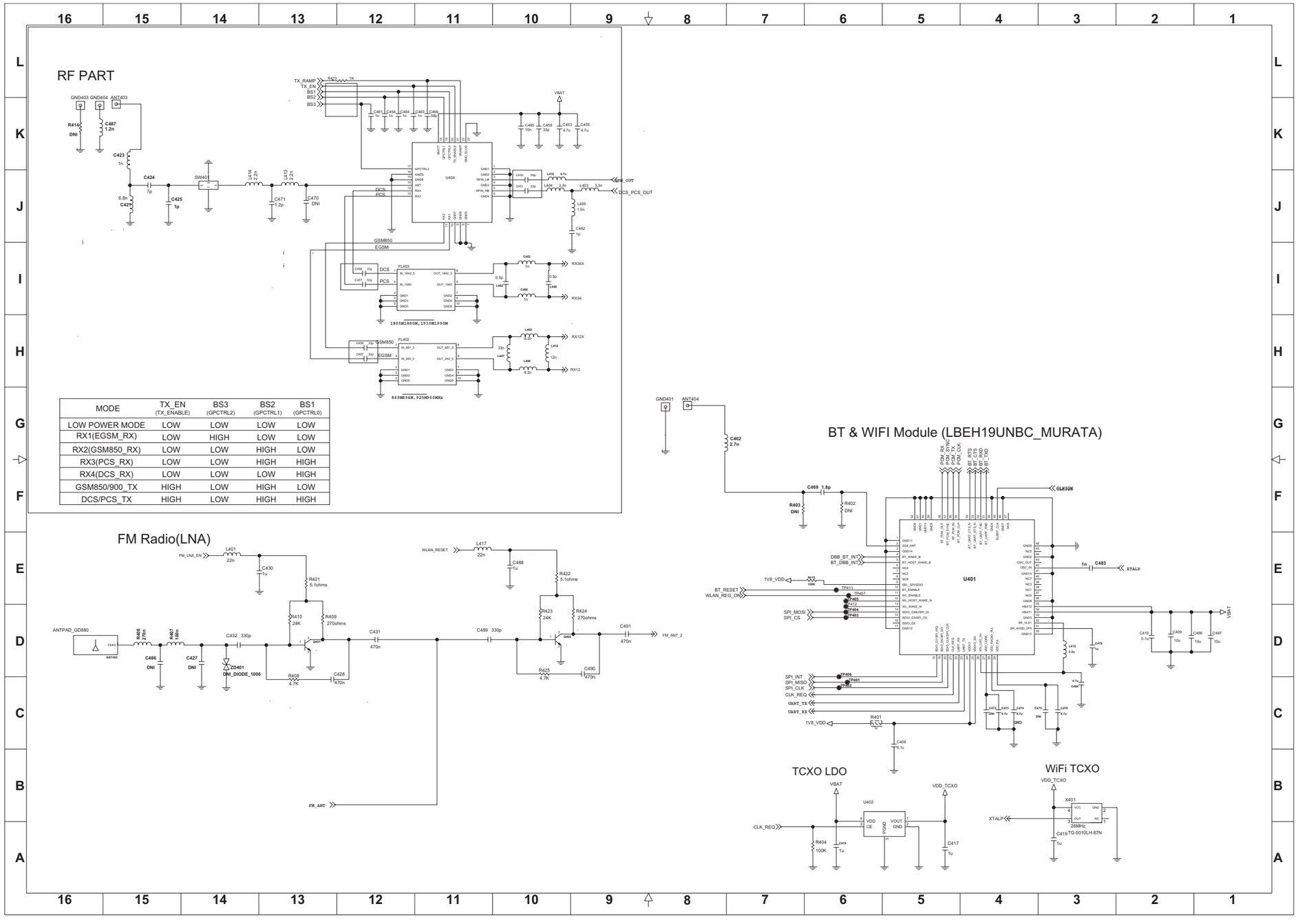
7. CIRCUIT DIAGRAM



7. CIRCUIT DIAGRAM



7. CIRCUIT DIAGRAM



MODE	TX_EN (TX_ENABLE)	BS3 (GPCTRL2)	BS2 (GPCTRL1)	BS1 (GPCTRL0)
LOW POWER MODE	LOW	LOW	LOW	LOW
RX1(EGSM_RX)	LOW	HIGH	LOW	LOW
RX2(GSM850_RX)	LOW	LOW	HIGH	LOW
RX3(PCS_RX)	LOW	LOW	HIGH	HIGH
RX4(DCS_RX)	LOW	LOW	LOW	HIGH
GSM850/900_TX	HIGH	LOW	HIGH	LOW
DCS/PCS_TX	HIGH	LOW	HIGH	HIGH

8. BGA PIN MAP

BGA IC pin check (U102)

▪ **Ball Diagram (Top View), PMB8810(A-GOLDRADIO+)**

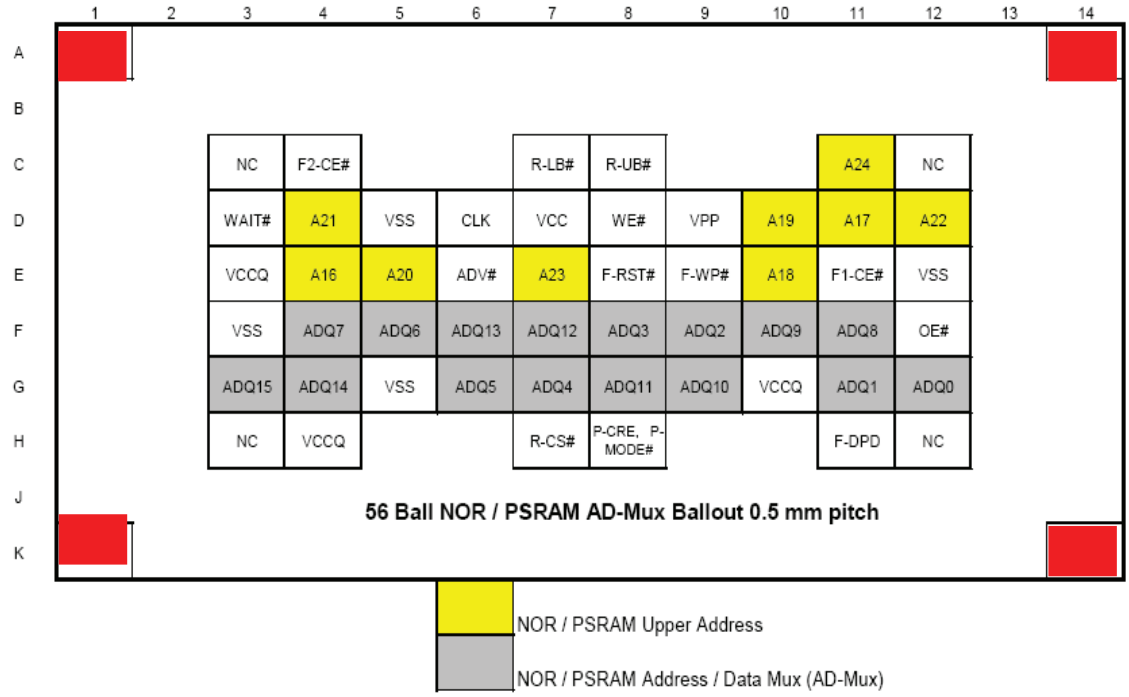
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	
16	VSSRF2	FE1	RX12X	RX12	RX34X	RX34	TMS	TCK	TDI	TRIG_IN	F32K	EPP	LSN	VBATSP	VDDNEG		16
15	TX1	TX2	VSSRF			VSSLO		TRST_n	TDO	FSYS_EN	OSC32K	EPN	LSP	VSSLSR	CP2	CP1	15
14	FE2	VDDTRX	VDET			VSSTRX	VBAT				VSSMS			VDD1V8CP	HSL	HSR	14
13	VRAMP	PABS	PABIAS			VSSRX	VDDRF2	VDDMS	MON1		RESET_N			VUMIC	MICN2	MICP2	13
12	VDDMMD	VDDTDC	PAEN		VSSDCO	VSSXO	VSSDIG	SWIF_TXRX	MON2	DMINUS			M0	VMIC	MICN1	MICP1	12
11	XO	XOX			VDDXO	FSYS2	FSYS1	DIGuP1	DIGuP_CLK	DPLUS		FMRINX	VDD_FMR	AGND	M2	M1	11
10	KP_IN1	KP_IN2	KP_IN3	KP_IN4	KP_IN5	KP_OUT5	DIGuP2	VRF1	VDD1V81	LEDFBP	VRTC	FMRIN		VPMU	ACD	VREF	10
9	KP_IN0	KP_OUT1	KP_OUT2	KP_OUT0	KP_OUT3	VDDFS	VDDIO1	VSSCORE2	VSSCORE3		LEDDRV	VUSB		ANAMON	ONOFF	VSS_PMU	9
8	I2S1_RX	I2S1_TX	I2S1_WA0	I2S1_CLK0	CIF_D7	VSSCORE1	VDDCORE	USIF2_TXD_MTSR	USIF2_CTS_n	VCORE	LEDFBN	VSIM	VBAT_PMU	VAUX	VSS_VIB	VIB	8
7	CIF_D3	CIF_D4	CIF_D6		CIF_VSYNC	CIF_HSYNC	CIF_PD	USIF2_RTS_n	USIF2_RXD_MRST	VDDIO2	VMMC	CS		VDD_SD1	SD1SW	VSS_SD1	7
6	CIF_D0	CIF_D1	CIF_D5		CIF_RESET	CLKOUT2	CIF_PCLK	MMCI_DAT1	WAIT_n	VSHNT	SENSEN	SENSEP			CSB	SD1_FB	6
5	I2C_SDA	I2C_SCL	CIF_D2				MMCI_DAT2			MMCI_DAT3				A/D13	VDD_EBU	VCHG	5
4	CLKOUT0	T2IN	MON3	DIF_RD		DIF_CS1	CC_RST	A19	A17	CS0_n	A/D9		A24	A20	WR_n	VDDCHG	4
3	USIF1_RTS_n	USIF1_RXD_MRST	DIF_WR	DIF_D3	DIF_CD	DIF_D7	CC_IO	MMCI_DAT0	A22	A/D0	A/D11	CS1_n	A/D4	A/D15	ADV_n	A23	3
2	USIF1_TXD_MTSR	USIF1_CTS_n	DIF_D4	DIF_RESET	DIF_D8	DIF_D2	CC_CLK	MMCI_CLK	A18	A/D1	A/D10	A/D5	A/D12	A/D7	A21	BFCLKO	2
1	VSSCORE4	DIF_D6	DIF_D5	DIF_D1	DIF_D0	DIF_HD	DIF_VD	MMCI_CMD	RD_n	A/D8	A/D2	A/D3	A/D6	A/D14	A16		1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	

: **not in use**

8. BGA PIN MAP

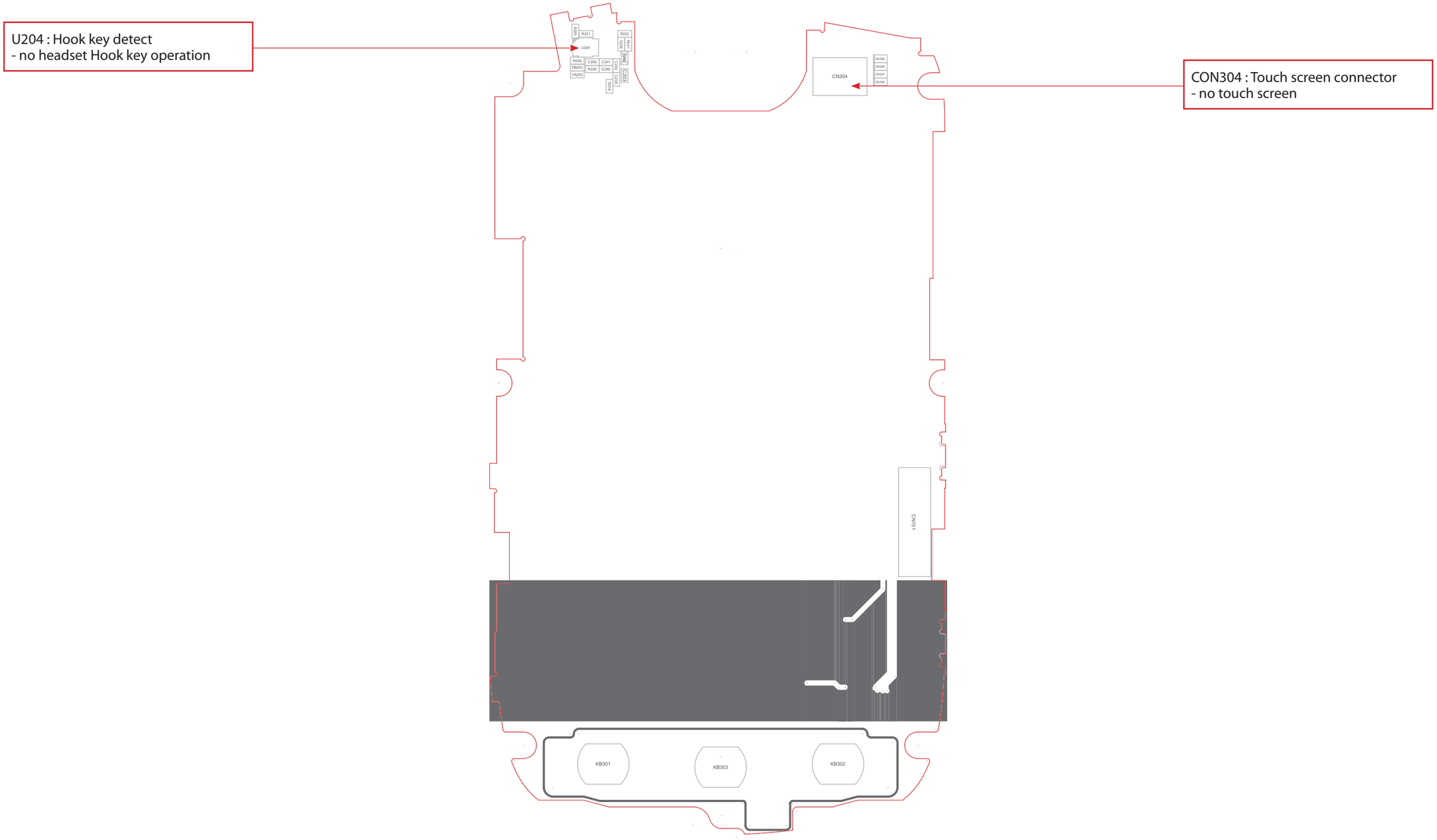
BGA IC pin check (U101)

▪ **Ball Diagram (Top View), PF38F5060M0Y3DF**



: not in use

9. PCB LAYOUT



LG-T310i-MAIN-SPFY0230301-1.0-TOP

9. PCB LAYOUT

ANT402 : FM radio Intenna contact
- no FM radio

U301 : Touch & Haptic IC
- no touch screen

U302 : ChargePump
- no LCD backlight

U201 : Charging IC
- no Battery Charge

CN202 : Battery Conn.
- no power On

S201 : T-Flash Socket
- no T-Flash Memory

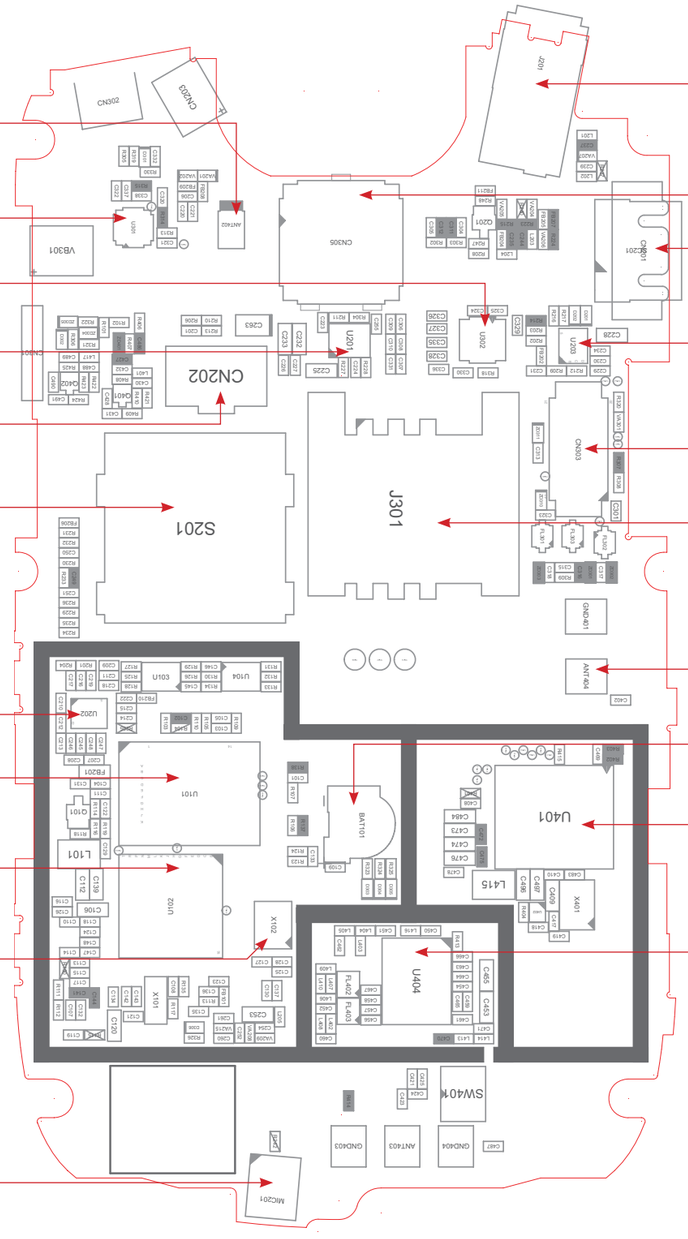
U202 : Audio Amp.
- no Sound

U101 : Memory
- no Booting

U102 : BB IC
- no Power On
- no Servive
- no FM radio

X102 : 26Mhz X-tal
- no Power On
- no Service

MIC201 : MAIN MIC
- no voice sending
- no voice recording



J201 : 3.5 pai ear jack
- no Earphone, headset MIC

CN305 : 2M Camera socket
- no Camera

CN201 : I/O conn.
- no USB Connection.
- no Serial Connection.

U203 : MUIC
- no Booting
- no USB/Serial Connection

CN303 : LCD Conn.
- no Display

J301 : SIM Conn.
- No SIM

ANT404 : BT Intenna contact
- no BT Connection

BAT101 : BackupCap.
- RTC Reset

U401 : BT/WIFI Module
- no BT Connection
- no WIFI Connection

U404 : PAM
- no Service
- RF Sensitivity & TX Power

LG-T310i-MAIN-SPFY0230301-1.0-BOT

10.ENGINEERING MODE

Engineering mode is designed to allow a service man/engineer to view and test the basic functions provided by a handset. The key sequence for switching the engineering mode on is "1809#*350# "Select. Pressing END will switch back to non-engineering mode operation. Use Up and Down key to select a menu and press 'select' key to progress the test. Pressing 'back key will switch back to the original test menu.

[1] BB TEST

[1-1] Battery Info

[1-1-1] BattInfo

[1-2] Bluetooth Test

[1-2-1] Enter Test Mode
[1-2-2] OnOff Test
[1-2-3] Headset Test
[1-2-4] BT Test1
[1-2-5] BT Test2
[1-2-6] Xhtml Compose Print
[1-2-7] Xhtml Print Test

[2] Model Version

[2-1] Version

[3] Eng Mode

[3-1] Cell environ.

[3-2] PS Layer Info

[3-2-1] Mobility
[3-2-2] RadioRes
[3-2-1] Gprs

[3-3] Layer1 Info

[3-4] Reset Information

[3-5] Memory Configurarion

[3-6] MemGenConf

[3-7] MemAllUse

[3-8] MemDetUse

[3-9] MemDump

[3-10] Change Frequency Band

[4] Call Timer

[5] Factory Reset

[6] MF TEST

[6-1] All Auto Test

[6-2] Backlight

[6-2-1] BacklightOn
[6-2-2] BacklightOff

[6-3] Audio

[6-3-1] Audio Test

[6-4] Vibrator

[6-4-1] VibratorOn
[6-4-2] VibratorOff

[6-5] LCD

[6-5-1] Auto LCD

[6-6] Key pad

[6-7] Mic Speaker

[6-8] Camera

[6-8-1] Camera Main Preview
[6-8-2] FlashOn
[6-8-3] FlashOff
[6-8-4] CameraFlashBunning

[6-9] FM Radio

[6-9-1] FM Radio Test

[7] Network selection

[7-1] Automatic

[7-2] GSM850

[7-3] EGSM

[7-4] DCS

[7-5] PCS

11. STAND ALONE TEST

11.1 Introduction

This manual explains how to examine the status of RX and TX of the model.

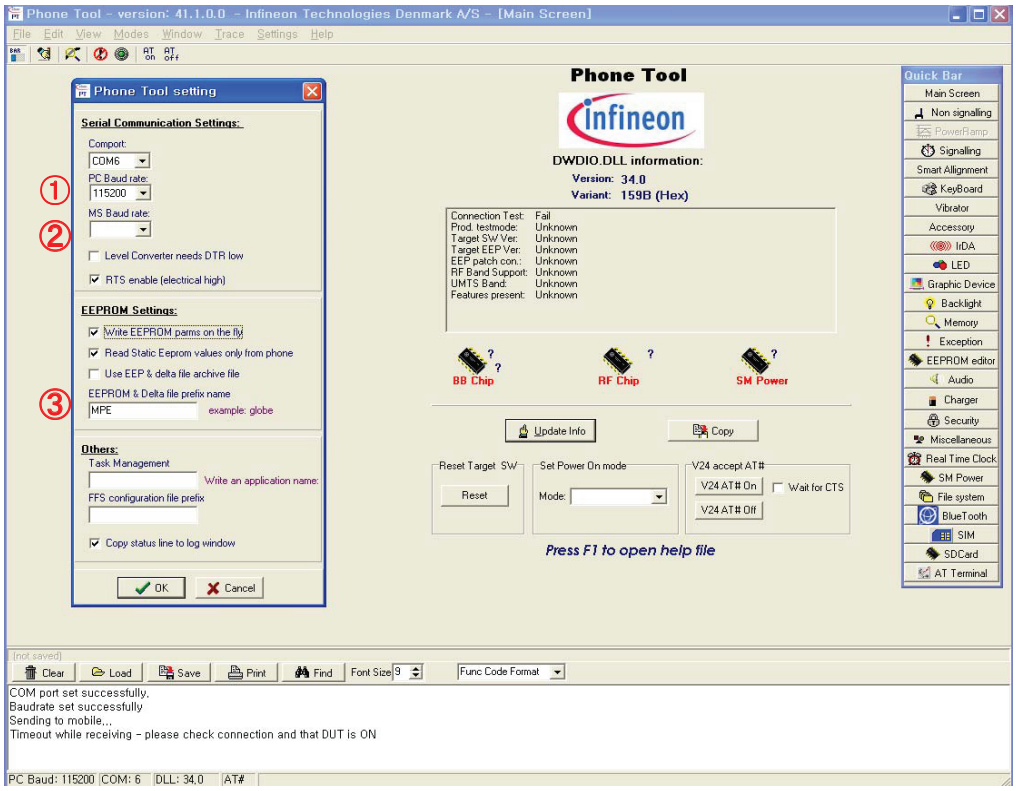
A. Tx Test

TX test - this is to see if the transmitter of the phones is activating normally.

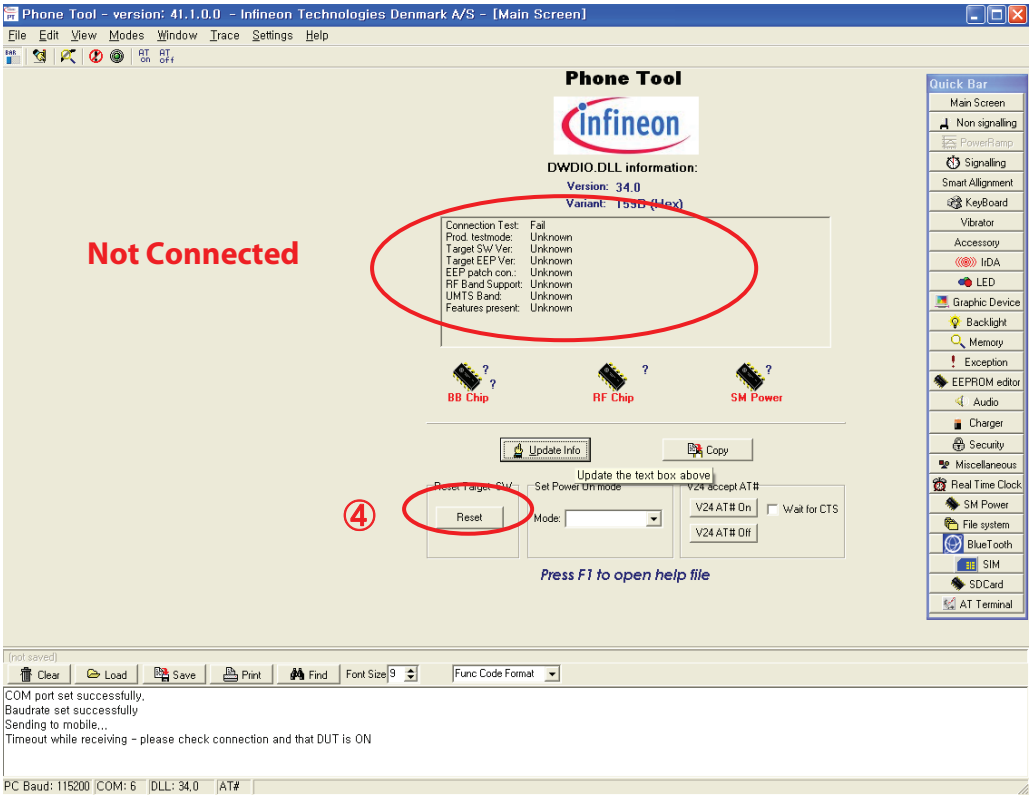
B. Rx Test

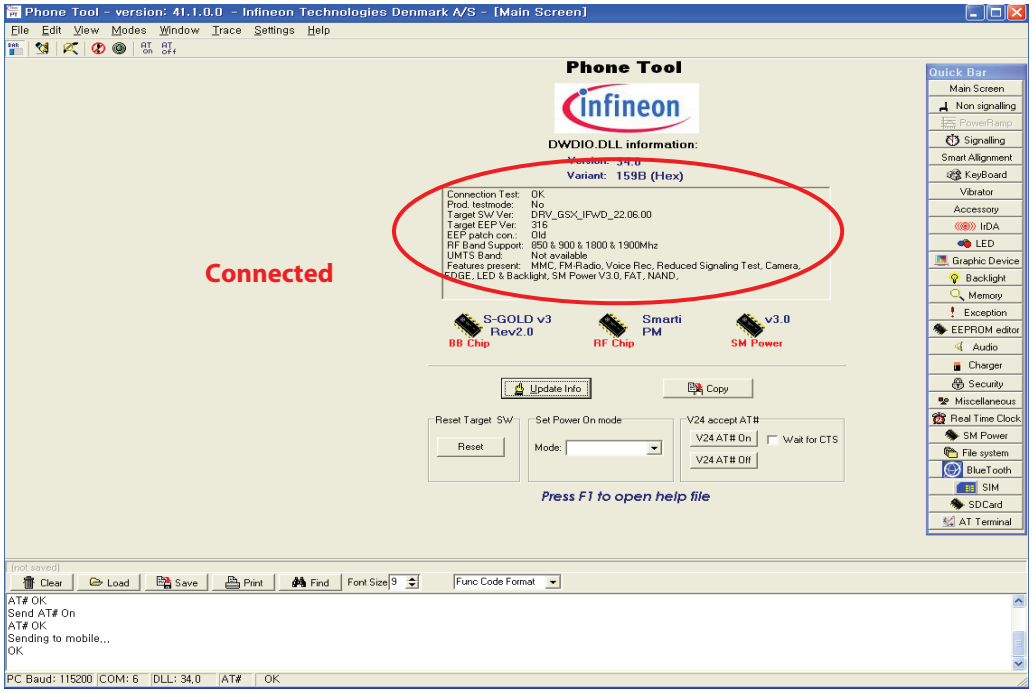
RX test - this is to see if the receiver of the phones is activating normally.

11.2 Setting Method

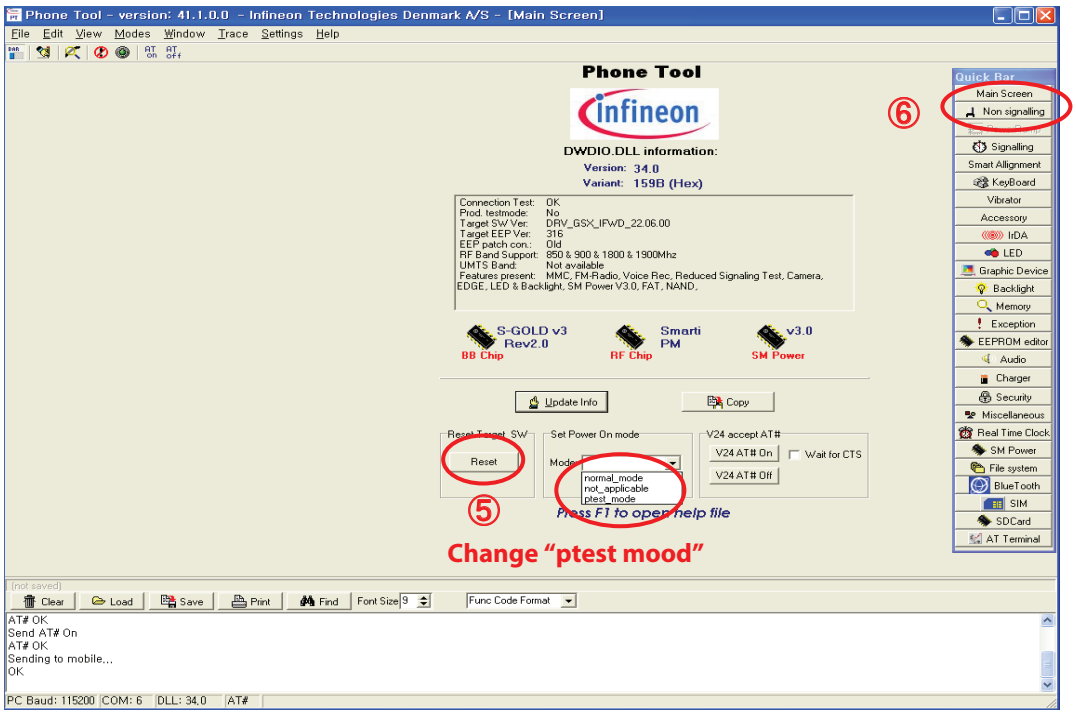


1. Set COM Port
2. Check PC Bau Rate
3. Confirm EEPROM & Delta file prefix name



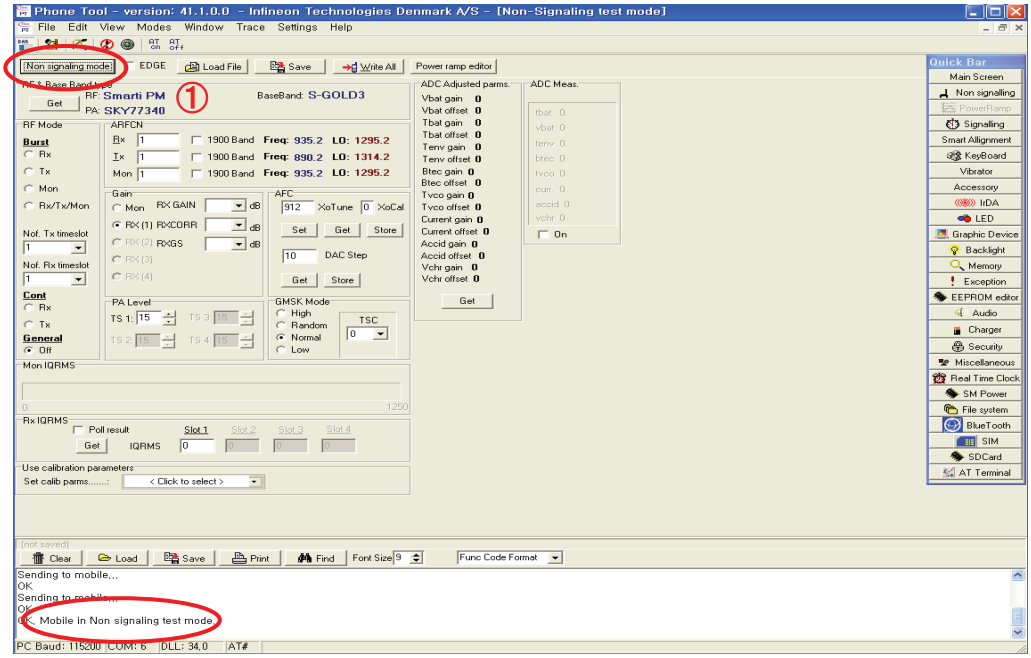


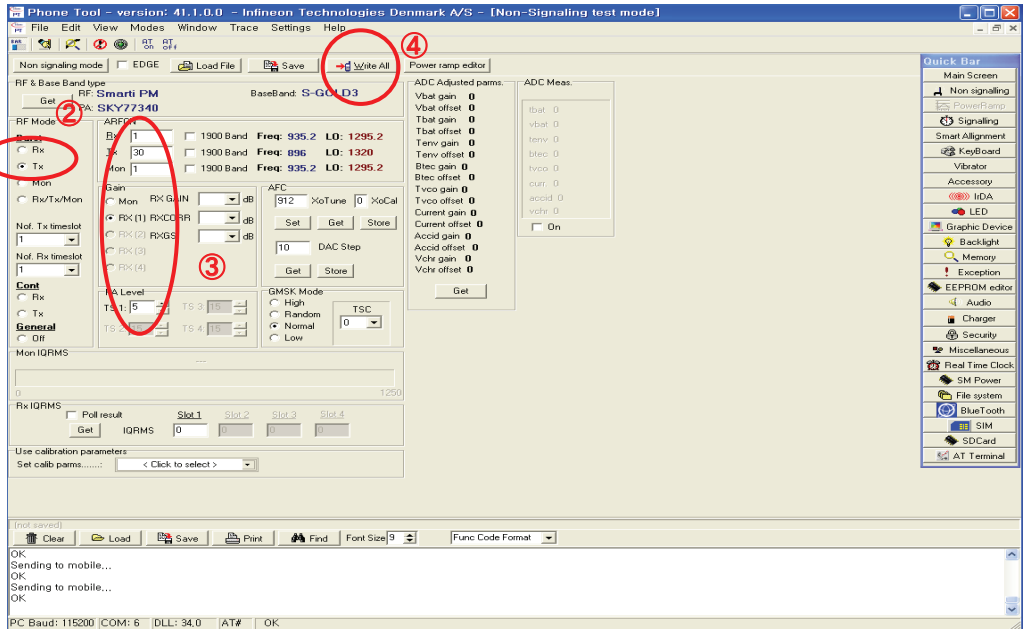
4. Click “Update Info” for communicating Phone and Test-Program



5. For the purpose of the Standalone Test, Change the Phone to "ptest mode" and then Click the "Reset" bar.
6. Select "Non signaling" in the Quick Bar menu. Then Standalone Test setup is finished.

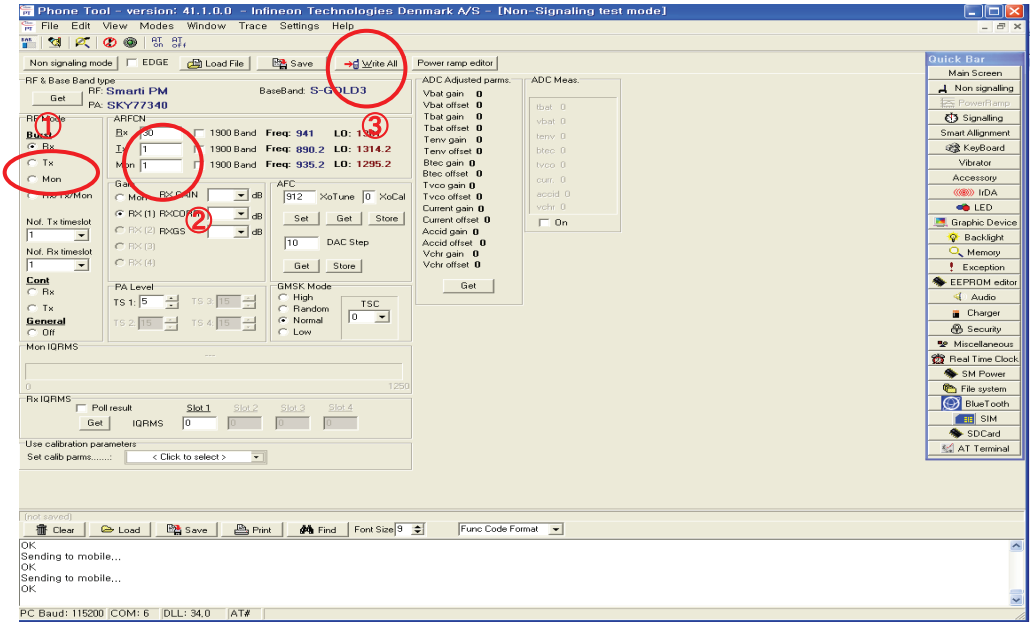
11.3 Tx Test

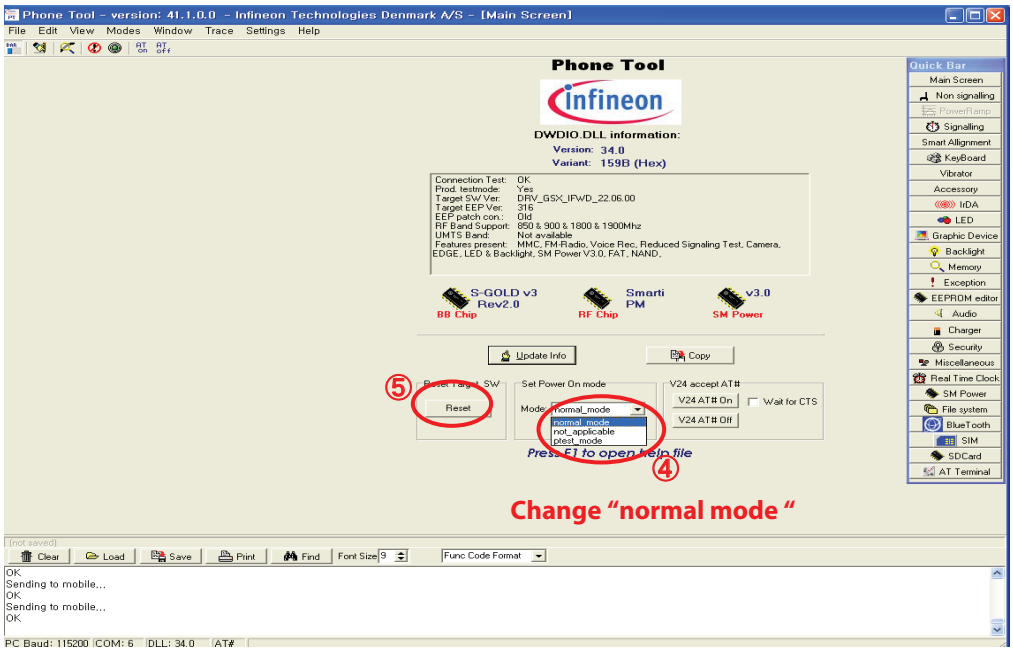




1. “Non signaling mode” bar and then confirm “OK” text in the command line.
2. Put the number of TX Channel in the ARFCN
3. Select “Tx” in the RF mode menu and “PCL” in the PA Level menu.
4. Finally, Click “Write All” bar and try the efficiency test of Phone.

11.4 Rx Test





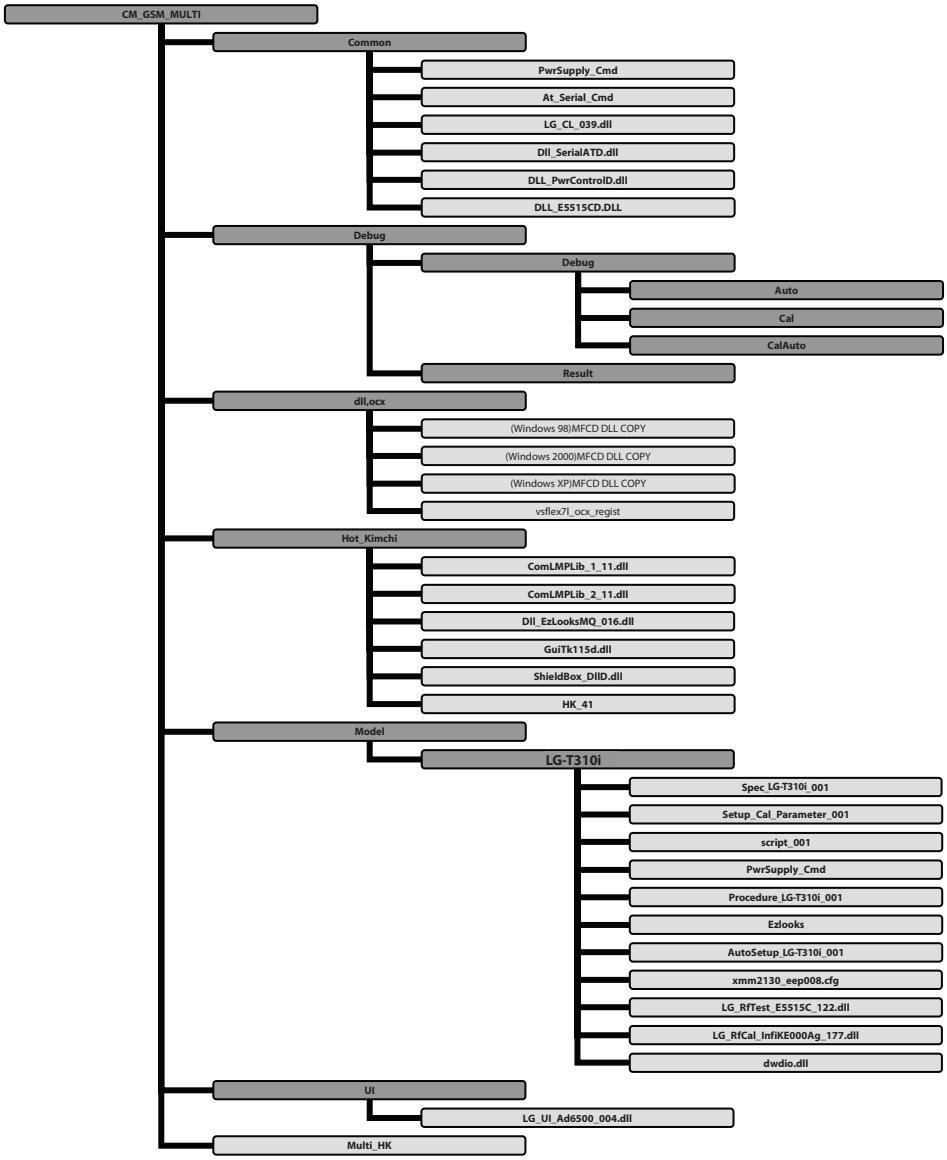
1. Put the number of RX Channel in the ARFCN.
2. Select “Rx” in the RF mode menu.
3. Finally, Click “Write All” bar and try the efficiency test of Phone.
4. The Phone must be changed “normal mode” after finishing Test.
5. Change the Phone to “normal mode” and then Click the “Reset” bar.

12.AUTO CALIBRATION

12.1 Overview

Auto-cal (Auto Calibration) is the PC side Calibration tool that perform Tx, Rx and Battery Calibration with Agilent 8960(GSM call setting instrument) and Tektronix PS2521G(Programmable Power supply).
Auto-cal generates calibration data by communicating with phone and measuring equipment then write it into calibration data block of flash memory in GSM phone.

12.2 Configuration of HotKimchi



12.3 Description of Basic File

12.3.1. Common

-. **LG_CL_039.dll** : Common logic dll, Module In Charge of Reading PID & S/W Version, Booting.
-. **Dll_SerialATD.dll** : Serial Communication Module From Phone by AT Command.
-. **DLL_PwrControlD.dll** : Communication Module From Power supply.
-. **DLL_E5515CD.DLL** : Communication Module From Agilent 8960(Test Set).
-. **At_Serial_Cmd.xml** : Definition File of AT Command.
-. **PwrSupply_Cmd.xml** : Definition File of Power supply command.

12.3.2 Debug

-. **Debug** - Cal : Result File of Calibration.
Auto : Result File of Auto Test.
CalAuto : Result File of Cal & Auto Test.

12.3.3 dll, ocx

-. **vsflex7l_ocx_regist :** Registration File for System use

-. **Windows XXX)MFCD DLL :** Registration File for System use

12.3.4 HotKimchi

-. **HK_40.exe** : Execute File, HK_XX → XX is File Version.
-. **ComLMPLib_1_11.dll** : Communication Module With PLC or Shield Box In Automation Rack.
Support to J&S Shield Box and Tescom TC-5981A.
-. **ComLMPLib_2_11.dll** : Communication Module With PLC or Shield Box In Automation Rack.
Support to J&S Shield Box and Tescom TC-5981A.
-. **Dll_EzLooksMQ_005.dll** : Communication Module with ezTray Installed In Local PC.
-. **GuiTk115d.dll** : control library
-. **ShieldBox_DllD.dll** : Communication with Shield Box. Support to Tescom TC-5952B.

12.3.5 Model

-. **LG_RfCal_InfiKE000Ag_177.dll** : Main Module of Calibration
-. **LG_RfTest_E5515C_122.dll** : Main Module of Auto Test
-. **Xmm2130_eep008.cfg** : Cal Data Save binary Module.
-. **AutoSetup_LG-T310i_100.xml** : RF TEST Setup Module.
-. **Ezlooks.xml** : Calibration ezLooks Item & Cal Spec Definition Module.
-. **Procedure_LG-T310i_001.xml** : RF TEST Procedure Definition Module.
-. **Script_001.xml** : RF TEST Setup & calibration Setup Module.
-. **Spec_LG-T310i_001.xml** : Definition Module of Auto Test Spec
-. **Setup_Cal_Parameter_001.xml** : Calibration Definition Module.

12.3.6 UI

-. LG_UI_Ad6500_002.dll : ADI Model UI Dll.

12.3.7 Multi_HK

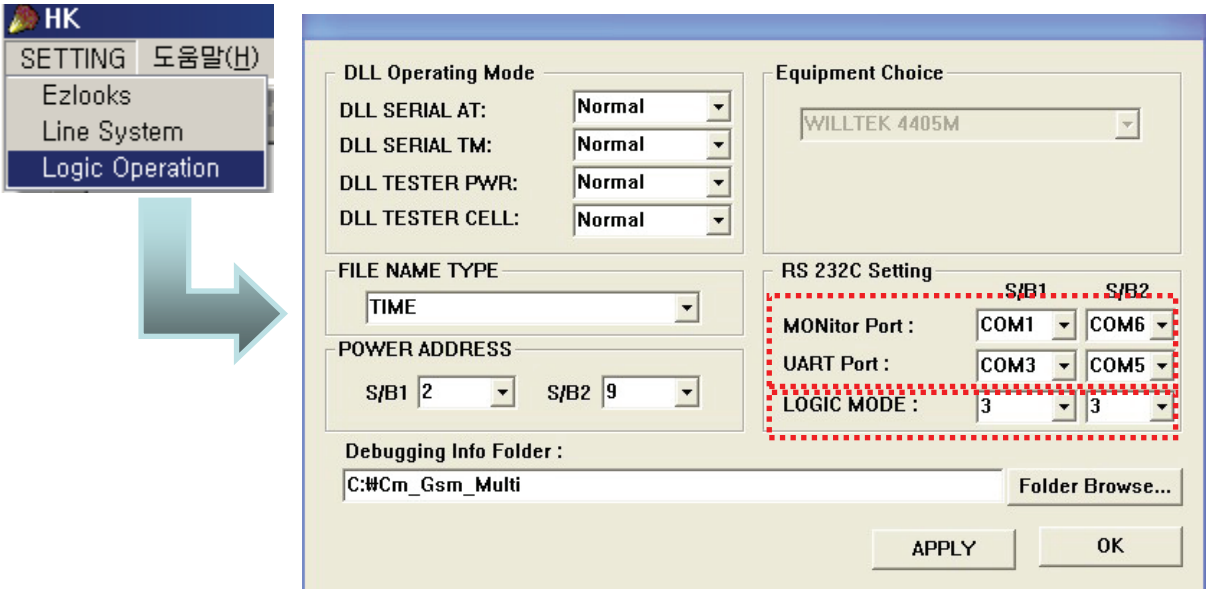
-. Registration File For System Setting.

1. Connect as Fig 6-2(RS232 serial cable is connected between COM port of PC and MON port of TEST JIG, in general)
2. Set the Power Supply 4.0V
3. Set the 3rd, 4th of DIP SW ON state always
4. Press the Phone power key, if the Remote ON is used, 1st ON state

12.4 Procedure

1. Copy the file to C:\Cm_Gsm_Multi
2. Copy the files of((Windows XXX)MFCD DLL, vsflex7l_ocx_regist to C:\Cm_Gsm_Multi\dll,ocx
3. Select MFCD DLL of your computer OS
4. Click on “vsflex7l_ocx_regist”
5. Click on “Multi_HK reg”
6. Connect as Fig 11-2 (RS232 serial cable is connected between COM port of PC, in general.)
7. . Run *HK_40exe* to start calibration.
8. Click “ Logic Operation” of “SETTING” menu bar

12.AUTO CALIBRATION

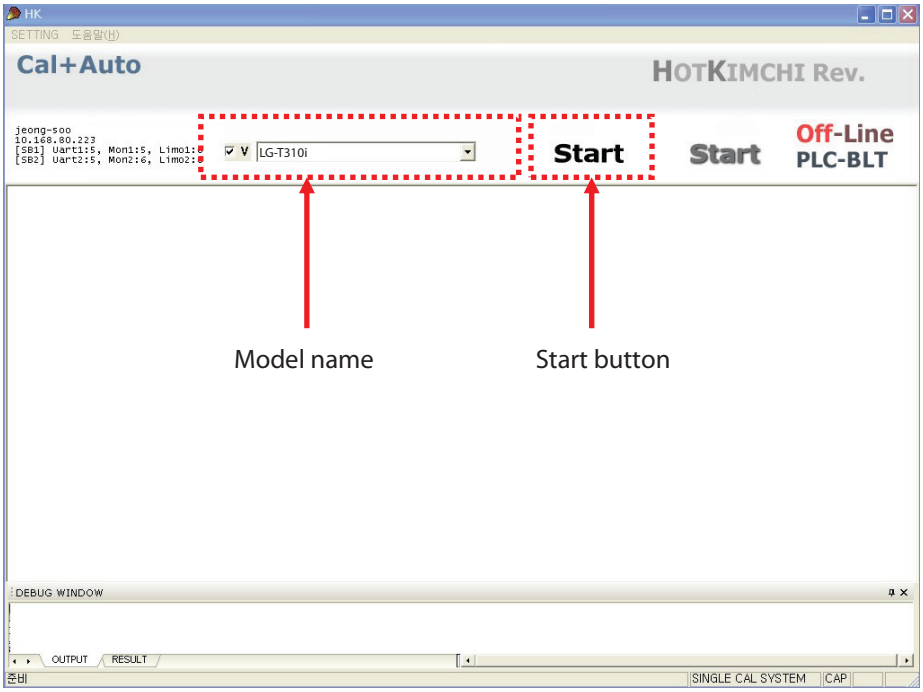


9. Set PORT (using RS232 cable) that PC can communicate with the phone

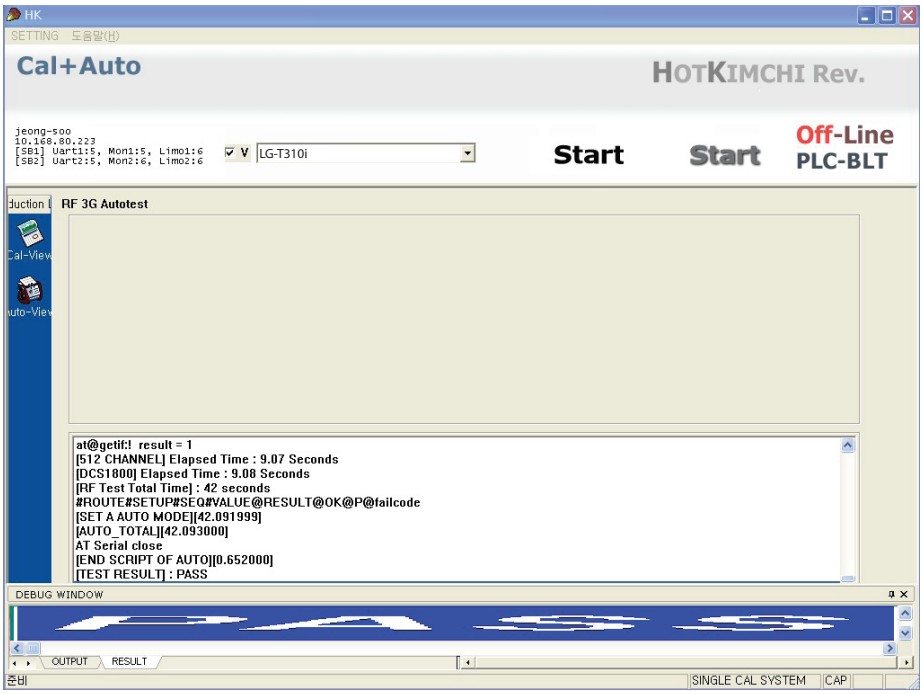
10. Select " LOGIC MODE" that you want

Logic mode: 1-> Calibration only
2-> Auto test only
3-> Cal & Auto

11. Select the model name “T310i”



12. Click “start” button



12.5 AGC

This procedure is for Rx calibration.
In this procedure, We can get RSSI correction value. Set band EGSM and press Start button the result window will show correction values per every power level and gain code and the same measure is performed per every frequency.

12.6 APC

This procedure is for Tx calibration.
In this procedure you can get proper scale factor value and measured power level.

12.7 ADC

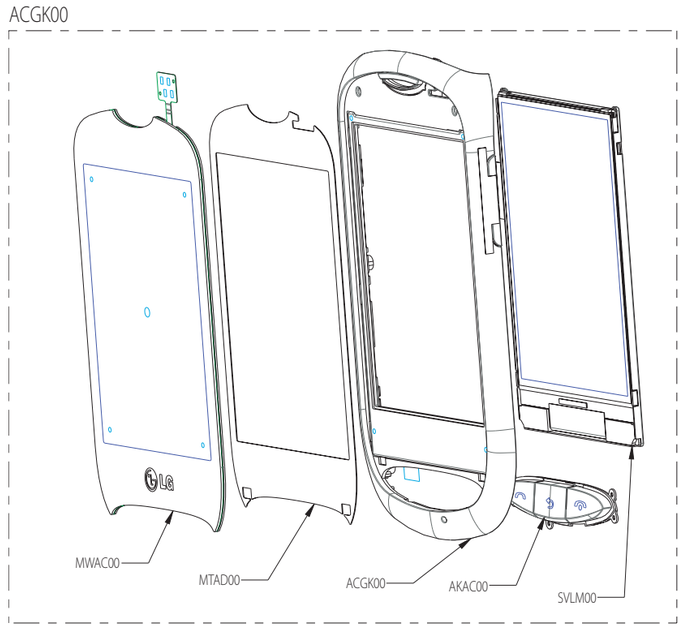
This procedure is for battery calibration.
You can get main Battery Config Table and temperature Config Table will be reset.

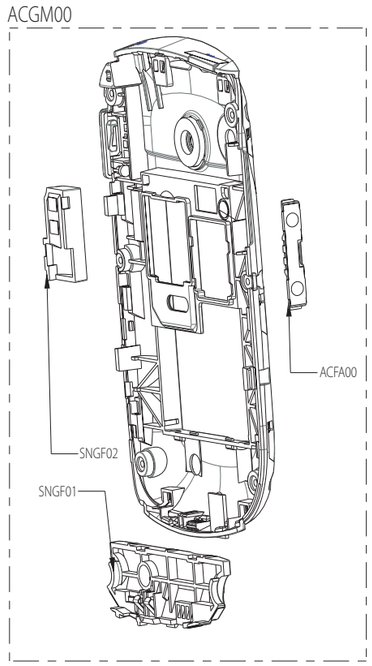
12.8 Target Power

BAND	Description	Low	Middle	High
GSM 850	Channel	128	191	251
	Frequency	824.2 MHz	836.8 MHz	848.8 MHz
	Max power	33 dBm	33 dBm	33 dBm
EGSM 900	Channel	975	37	124
	Frequency	880.2 MHz	897.4 MHz	914.8 MHz
	Max power	33 dBm	33 dBm	33 dBm
DCS1800	Channel	512	699	885
	Frequency	1710.2 MHz	1747.6 MHz	1784.8 MHz
	Max power	30 dBm	30 dBm	30 dBm
PCS 1900	Channel	512	661	810
	Frequency	1850.2 MHz	1880 MHz	1909.8 MHz
	Max power	29.3 dBm	29.3 dBm	29.3 dBm

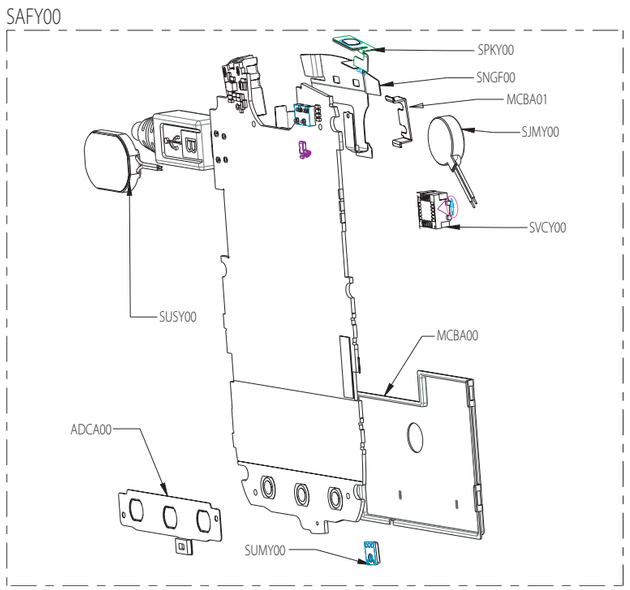
13. EXPLODED VIEW & REPLACEMENT PART LIST

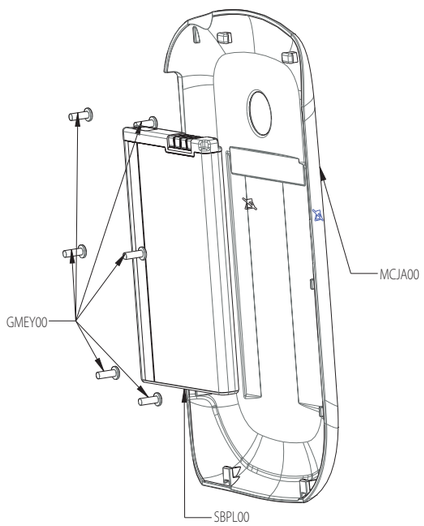
13.1 EXPLODED VIEW





Location	Description
SAFY00	PCB Assembly,Main
ADCA00	DOME ASSY,METAL
MCBA00	CAN,SHIELD
SJMY00	Motor,DC
SNGF00	Antenna,Helical
SPKY00	PCB,Sidekey
SUSY00	Speaker,Dual Mode
SVCY00	Camera Module
MCBA01	Can,Shield
SUMY00	Microphone,Condenser
ACGM00	COVER ASSY,REAR
ACFA00	CONTACT ASSY,SIDE BUTTON
SNGF01	Antenna,Helical
SNGF02	Antenna,Helical
ACGK00	Cover Assembly,Front
MTAD00	TAPE,WINDOW
AKAC00	Keypad Assembly,Main
MWAC00	WINDOW,LCD
SVLM00	LCD Module
GMEY00	Screw,Machine
MCJA00	COVER,BATTERY
SBPL00	Mobile Phone Battery Li-Ion





13.2ReplacementParts <Mechanic component>

Note: ThisChapterisusedforreference,Partorderisordered bySBOMstandardonGCSC

Level	LocationNo.	Description	PartNumber	Spec	Remark
1	AAAY00	AdditionAssembly	AAAY0513012☞10	LG-T310iTFHBKBK:Black-	
1	AGF000000	PackageAssembly	APAY0150018☞7	LG-T310iCLABKZZ:WithoutColorEU1W_LGT310i_SPN_6AL_CLASTD	
2	MBAD00	Bag,Vinyl	MBAD0005204	COMPLEXLG-LX260SPRAGZZ:WithoutColor-	
2	MBEE00	Box,Master	MBEE0061001	COMPLEXGD510CZESVZZ:WithoutColor-	
2	MBEF00	Box,Unit	MBEF0149106	COMPLEXLG-T310iTURBKZZ:WithoutColorCOMPLEX,EU1W_LG-T310i_SPN_SPNOpen	
2	MLAC00	Label,Barcode	MLAC0004541	COMPLEXHB620KPNBKZZ:WithoutColor-	
2	MLAJ00	Label,MasterBox	MLAJ0004402	COMPLEXCG300CGRZZ:WithoutColorLABEL,MASTER BOX(forCGRTDR2VER.mbox_label)	
2	MLAZ00	Label	MLAZ0050901	COMPLEXKU990GBRBKZZ:WithoutColor-	
2	MPCY	Pallet	MPCY0021701	COMPLEXKC910AUSTNZZ:WithoutColor-	
1	APEY	PhoneAssembly	APEY0914109☞6	LG-T310iTFHBKBK:Black-	
2	ACGY	CoverAssembly, EMS	ACGY0092108☞4	LG-T310iTFHBKBK:Black-	
3	ACGM	CoverAssembly, Rear	ACGM0161302☞16	LG-T310VIVBKRD:Red-	
4	ACFA	ContactAssembly, SideButton	ACFA0000302	i-CommonZZZBKZZ:WithoutColor2ButtonType	
4	MBJZ	Button	MBJZ0033802	COMPLEXLG-T310VIVBKRD:RedMOLD,PCLUPOYSC-1004A,,,,,	
4	MCCZ	Cap	MCCZ0040602	COMPLEXLG-T310VIVBKBK:Black-	
4	MCJN	Cover,Rear	MCJN0122702	COMPLEXLG-T310VIVBKRD:RedMOLD,PCLUPOYSC-1004A,,,,,	
4	MDAY00	Decor	MDAY0072901	COMPLEXLG-T310TURWAZZ:WithoutColorCOMPLEX,(empty),,,,,	
4	MHK000000	Sheet	MHK63305201	COMPLEXLGT310.ATURBKBK:Black-	
4	MLAB	Label,AfterService	MLAB0001102	COMPLEXC2000CGRSVWA:WhiteC2000USASVDIA4.0 PRINTING,	
4	MPBJ00	Damper,Motor	MPBJ0076201	COMPLEXLG-T310VIVBKZZ:WithoutColor-	
4	MPBT00	Damper,Camera	MPBT0095501	COMPLEXLG-T310VIVBKZZ:WithoutColor-	
4	MPBU00	Damper,Connector	MPBU0103101	COMPLEXLG-T310VIVBKZZ:WithoutColor-	

13. EXPLODED VIEW & REPLACEMENT PART LIST

Level	LocationNo.	Description	PartNumber	Spec	Remark
4	MPBZ00	Damper	MPBZ0324501	COMPLEXLG-T310VIVBKZZ:WithoutColorCOMPLEX,(empty),,,,,	
4	MTAB00	Tape,Protect	MTAB0401401	COMPLEXLG-T310VIVBKZZ:WithoutColor-	
4	MTAK00	Tape,Camera	MTAK0039801	COMPLEXLG-T310VIVBKZZ:WithoutColor-	
4	MWAE00	Window,Camera	MWAE0062001	COMPLEXLG-T310VIVBKZZ:WithoutColor-	
3	ACGV	CoverAssembly, Bar	ACGV0019210☞7	LG-T310TURWRWR:WINEREDT310USPFILM	
4	ACGK	CoverAssembly, Front	ACGK0162304☞11	LG-T310VIVWRBK:Black-	
5	MBG000001	Button	MBJZ0033704	COMPLEXLG-T310VIVWRWR:WINERED-	
5	MCK032702	Cover,Front	MCJK0130004	COMPLEXLG-T310VIVWRWI:WINE-	
5	MDAY00	Decor	MDAY0072801	COMPLEXLG-T310VIVBKBK:Black-	
5	MFBZ00	Filter	MFBZ0019201	COMPLEXLG-T310VIVBKZZ:WithoutColor-	
5	MFEZ00	Frame	MFEZ0031101	COMPLEXLG-T310VIVBKZZ:WithoutColor-	
5	MGAZ00	Gasket	MGAZ0104601	COMPLEXLG-T310VIVBKGD:GoldCOMPLEX,(empty),,,,,	
5	MPBG00	Damper,LCD	MPBG0110101	COMPLEXLG-T310VIVBKZZ:WithoutColor-	
5	MTAA00	Tape,Decor	MTAA0223501	COMPLEXLG-T310VIVBKZZ:WithoutColor-	
5	MTAB00	Tape,Protect	MTAB0401301	COMPLEXLG-T310VIVBKZZ:WithoutColor-	
5	MTAD00	Tape,Window	MTAD0127801	COMPLEXLG-T310VIVBKZZ:WithoutColor-	
5	MTAZ00	Tape	MTAZ0316601	COMPLEXLG-T310VIVBKZZ:WithoutColor-	
4	AKAC	KeypadAssembly, Main	AKAC0014405	LG-T310VIVWRBK:Black-	
4	MTAB00	Tape,Protect	MTAB0448401	COMPLEXLG-T310VIVBKZZ:WithoutColorCOMPLEX,(empty),,,,,	
4	MTAB	Tape,Protect	MTAB0449401	COMPLEXLG-T310VIVBKZZ:WithoutColorCOMPLEX,(empty),,,,,	
4	MTAZ00	Tape	MTAZ0364201	COMPLEXLG-T310VIVBKGN:GreenCOMPLEX,(empty),,,,,	
4	MWAC00	Window,LCD	MWAC0144901	COMPLEXLG-T310VIVBKZZ:WithoutColor-	
3	GMEY00	Screw,Machine	GMEY0014301	GMEY0014301BH+1.4mM3.5mMMSWRNIPLTN-KUMGANGSCREWCO.,LTD	
2	MLAA00	Label,Approval	MLAA0062301	COMPLEXKB770DEUBKZZ:WithoutColor-	

13.2ReplacementParts
<Main component>

Note: ThisChapterisusedforreference,Partorderisordered bySBOMstandardonGCSC

Level	LocationNo.	Description	PartNumber	Spec	Remark
2	ENSY00	CardSocket	ENSY0015401	SCHH1A0200SCHC1A0400,9PIN,ETC,,mm,SDAdaptorforTFRALPSELECTRICCO.,LTD.	
2	ENSY00	Socket,Card	*S*ENSY0021201	AXA4A5011SD9PSTRAIGHTSMDR/TPAdoptorPANASONICELECTRICWORKSKOREACO.,LTD	
4	SNGF00	Antenna,Helical	SNGF0061402	HIR-02A39-0000AA3.0,-5dBd,internal,GSM850/900/1800/1900,QUAD,-5.0,50,3.0E.M.WCO.,LTD.	
4	SNGF01	Antenna,Helical	SNGF0061501	712789.0001SINGLE-5DB50OHM3LAIRDTECHNOLOGIESKOREA	
4	SVLM00	LCDModule	SVLM0040001	LS028Q3UW01Main,2.8,QVGA,47.4x70.21x1.9t,262K,TFT,TM,NT35751,SHARPCORPORATION.	
3	SAFY00	PCBAssembly,Main	SAFY0401001	LG-T310iTFHBKMAIN,A	
2	SMZY00	IC,MemoryCard, MICROSD	SMZY0017802	SDSDQ-2048-974SDSDQ-2048-974,2GB/MICROSD/MLC1DIESANDISKCORPORATION	
2	SMZY00	IC,MemoryCard, MINISD	*S*SMZY0027202	SD-C02G2CYBMicroSDCard/2GB(MLCNAND16Gbx1),ModuleAssembly,TOSHIBA	
2	SMZY00	IC,MemoryCard, MICROSD	*S*SMZY0018303	CS2GLC-02B2GBYTE2.7VTO3.6VMICROSDCARD15.0x11.0x0.7MMBK8P-LGELECTRONICSINC.	
2	SMZY00	IC,MemoryCard, MICROSD	*S*SMZY0017703	KT02GSMLAMKT02GSMLAM,2GB/MICROSD/MICRONMLC2DIESKINGMAXDIGITALINC.	

13. EXPLODED VIEW & REPLACEMENT PART LIST

13.3 Accessory

Note: ThisChapterisusedforreference,Partorderisordered bySBOMstandardonGCSC

Level	LocationNo.	Description	PartNumber	Spec	Remark
2	SBPL00	MobilePhoneBatteryLi-Ion	SBPL0098201	LGIP-430N-WW-TOLGIP-430N-WW-SANYO,3.7V,900mAh,1CELL,PRISMATIC,463450,INNERPACK,WWTOCADDONGHWA	
2	SGDY00	Accessory, DataCable	SGDY0018001	LG0029LG0029MicroUSB,0.8Mningbobroadtelecommunicationco.,ltd	
2	SGEY00	Earphone,Stereo	SGEY0003744	EMB-LGE004MSKB3mW16OHM115DB85HZTO126HZ1MBLACK3.5LTYPESTEREO4POLEPLUG-CRESYNCO.,LTD	
2	SSAD00	Adapters	SSAD0034501	STA-U35ER90Vac~264Vac4.8V400mA5060CENONENONE-SUNLINELECTRONICSCO.,LTD	
2	SSAD00	Adapters	*S*SSAD0034502	90Vac~264Vac4.8V400mA5060CENONENONE-	
2	SSAD00	Adapters	*S*SSAD0034504	STA-U35ES90Vac~264Vac4.8V400mA5060CENONENONE-SALCOMPOY	
2	SSAD00	Adapters	*S*SSAD0034503	STA-U35ED90Vac~264Vac4.8V400mA5060CENONENONE-DONGDOELECTRONICSCO.,LTD	